



**MODEL:
HYPER-EHL**

**Pico-ITX SBC Supports Intel® Celeron® J6412/N6210
on-board SoC with 4GB LPDDR4x, HDMI,
iDPM, M.2, 2.5GbE LAN, PCIe x4 Slot, COM,
iSATA 6Gb/s, USB 3.2 Gen 2, and RoHS**

User Manual

Revision

Date	Version	Changes
August 14, 2023	1.00	Initial release

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Manual Conventions



WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.



CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.



NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

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Chapter

1

Introduction

HYPER-EHL

1.1 Introduction

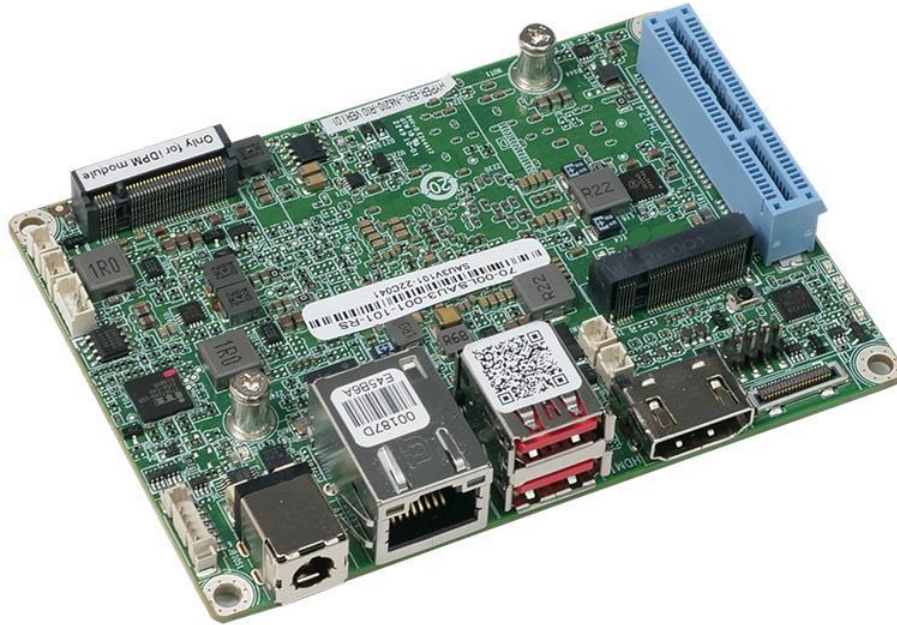


Figure 1-1: HYPER-EHL

The HYPER-EHL series is a single board computer in Pico-ITX form factor. It is powered by Intel® Celeron® J6412 on-board SoC or Intel® Celeron® N6210 on-board SoC. It supports on-board 4GB 3200 MHz LPDDR4X (system max. 8GB).

The HYPER-EHL series includes HDMI and IEI iDPM for dual independent display. It provides one 2.5GbE interface through the Intel® I225V controller. Expansion and I/O include one PCIe x4 slot, one M.2 slot, one COM port, one iSATA 6Gb/s connector, two USB 3.2 Gen 2 and two USB 2.0.

1.2 Features

Some of the HYPER-EHL motherboard features are listed below:

- Support Intel® Atom® x6000 series / Pentium® / Celeron® processor (Elkhart Lake platform)
Intel® Celeron® J6412 on-board SoC
(up to 2.6GHz, quad-core, 1.5M cache, TDP=10W)
Intel® Celeron® N6210 on-board SoC
(up to 2.6GHz, dual-core, 1.5M cache, TDP=6.5W)
- On-board 4GB 3200 MHz LPDDR4X (system max. 8GB)
- One 2.5GbE via Intel® I225V controller
- Dual independent display by HDMI and IEI iDPM
- One iSATA 6Gb/s connector
- Two USB 3.2 Gen 2 ports and two USB 2.0
- One M.2 M-key slot with PCIe x2 and USB 2.0 signal
- One PCIe x4 slot
- One serial port
- RoHS compliant

HYPER-EHL

1.3 Connectors

The connectors on the HYPER-EHL are shown in the figure below.

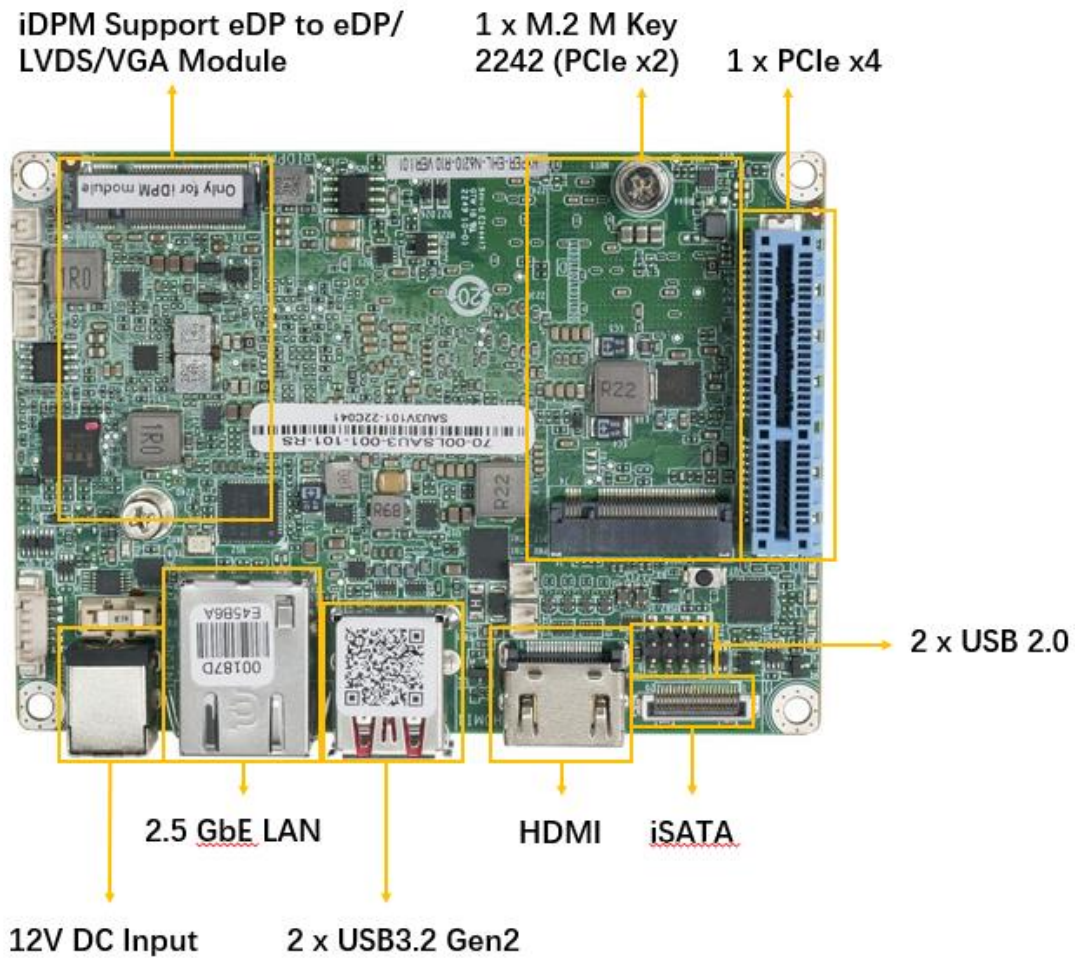


Figure 1-2: Connectors

1.4 Dimensions

The main dimensions of the HYPER-EHL are shown in the diagram below.

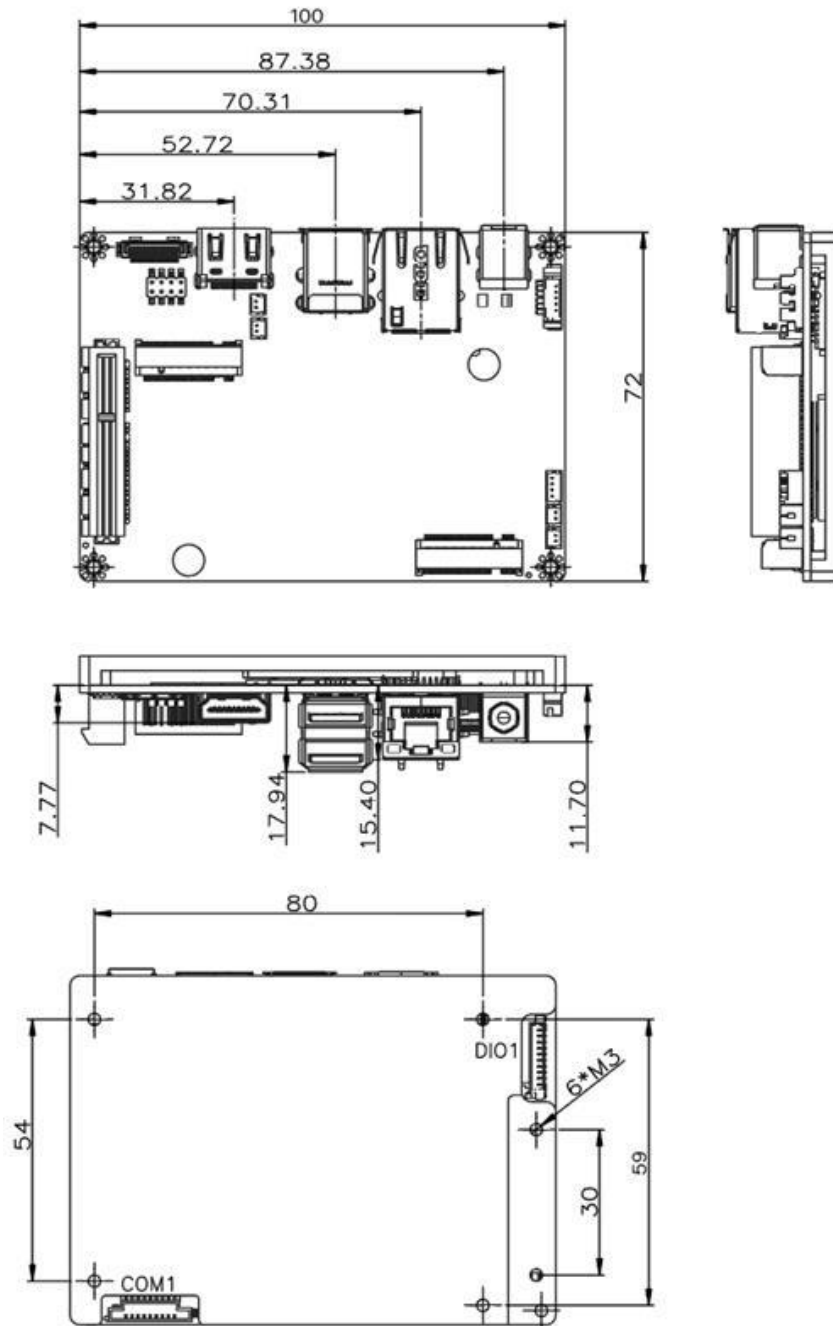


Figure 1-3: HYPER-EHL Dimensions (mm)

HYPER-EHL

1.5 Data Flow

Figure 1-4 shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

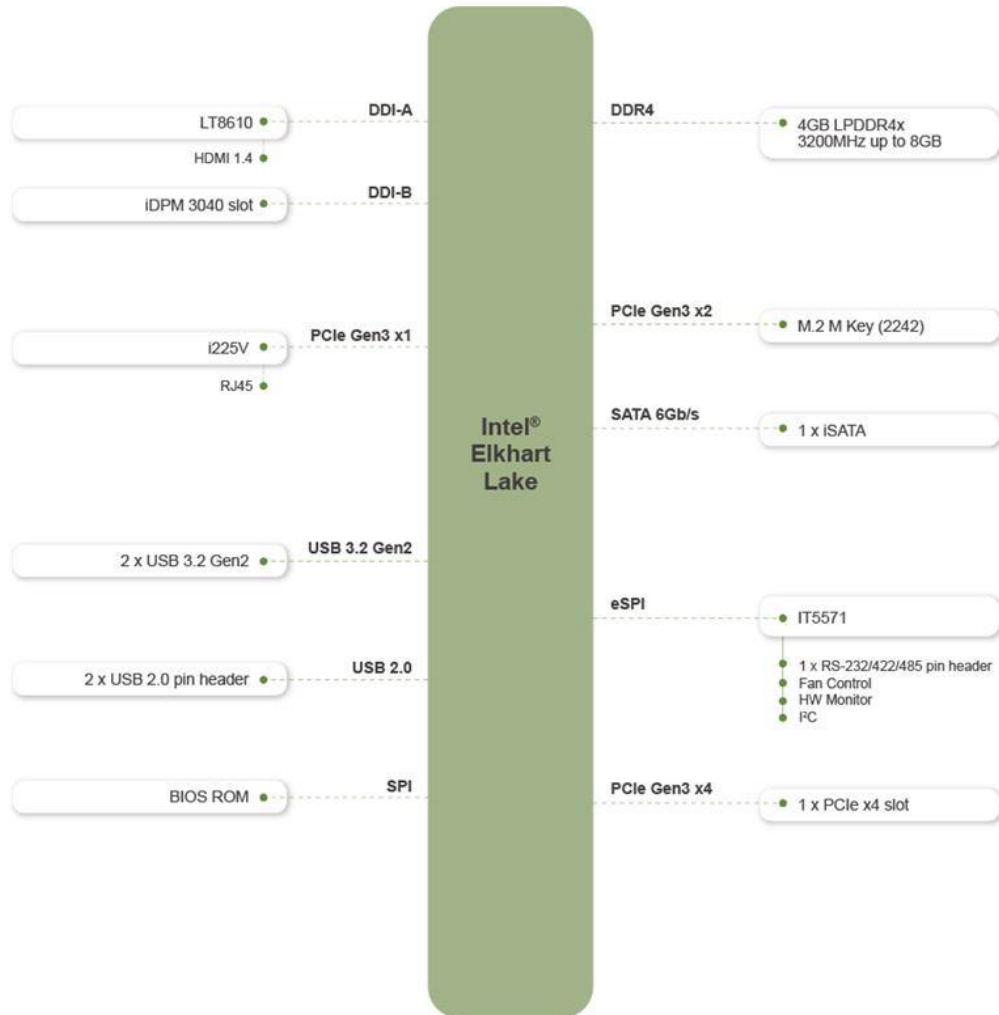


Figure 1-4: Data Flow Diagram

1.6 Technical Specifications

The HYPER-EHL technical specifications are listed below.

Specification/Model	HYPER-EHL
Form Factor	Pico-ITX
CPU Supported	Support Intel® Atom® x6000 series / Pentium® / Celeron® processor (Elkhart Lake platform) Intel® Celeron® J6412 on-board SoC (up to 2.6GHz, quad-core, 1.5M cache, TDP=10W) Intel® Celeron® N6210 on-board SoC (up to 2.6GHz, dual-core, 1.5M cache, TDP=6.5W)
Memory	On-board 4GB 3200 MHz LPDDR4X (system max. 8GB)
Graphics Engine	Intel® UHD Graphics (Gen11)
Display Output	Dual independent display 1 x HDMI 1.4 (up to 4096 x 2160 @ 30Hz) 1 x IEI iDPM 3040 slot (only for IEI eDP/LVDS/VGA module)
Ethernet Controllers	1 x 2.5GbE via Intel® I225V controller
BIOS	AMI UEFI BIOS
Watchdog Timer	Software programmable supports 1~255 sec. system reset
Expansions	1 x M.2 2242 M key (PCIe x2 & USB 2.0) 1 x PCIe x4 slot (PCIe Gen3 x4 signal, x4 or x2+x2 or 1+x1+x1+x1)
I/O Interface Connectors	
Digital I/O	8-bit digital I/O
Ethernet	One RJ-45 GbE port
Front Panel	1 x Power button connector (1x2 pin, p=1.25) 1 x Reset button connector (1x2 pin, p=1.25)
I²C	One 4-pin wafer connector
Serial ATA	1 x iSATA 6Gb/s

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Specification/Model	HYPER-EHL
Serial Ports	1 x RS-232/422/485 (1x9 pin, p=1.25)
USB Ports	2 x USB 3.2 Gen 2x1 Type-A (10Gb/s) 2 x USB 2.0 (2x4 pin, p=2.0)
Environmental and Power Specifications	
Power Supply	AT/ATX power supply
Power Consumption	12V@ 2.07A (Intel® Celeron® J6412 CPU with 4 GB 3200 MHz LPDDR4x memory, max. loading, EuP mode enabled)
Operating Temperature	0°C ~ 60°C
Storage Temperature	-30°C ~ 70°C
Operating Humidity	5% ~ 95% (non-condensing)
Physical Specifications	
Dimensions	100 mm x 72 mm
Weight (GW/NW)	600g / 250g

Table 1-1: HYPER-EHL Specifications

Chapter

2

Packing List

HYPER-EHL

2.1 Anti-static Precautions



WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- **Wear an anti-static wristband:** Wearing an anti-static wristband can prevent electrostatic discharge.
- **Self-grounding:** Touch a grounded conductor every few minutes to discharge any excess static buildup.
- **Use an anti-static pad:** When configuring any circuit board, place it on an anti-static mat.
- **Only handle the edges of the PCB:** Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the HYPER-EHL is unpacked, please do the following:

- Follow the anti-static guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

2.3 Packing List



NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the HYPER-EHL was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

The HYPER-EHL is shipped with the following components:

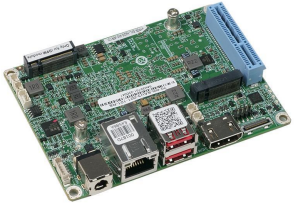





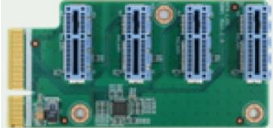

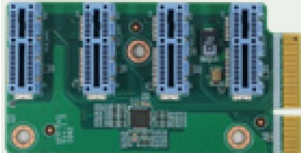
Quantity	Item and Part Number	Image
1	HYPER-EHL single board computer	
2	iSATA cable	
1	Quick installation guide	<p><small>Pico-ITX SBC Supports Intel® Celeron® J6412NE19 on-board SoC with 4GB LPDDR4x, H265, GPM, 2.5GBE LAN, M.2, PCM 48 Bits, SATA, HDMI, COM, USB 3.2 Gen 2, and Ports</small></p> <p>HYPER-EHL Quick Installation Guide Version 1.0 May 16, 2023</p> <p>Package List: HYPER-EHL package includes the following items:- • 1 x HYPER-EHL single board computer • 1 x iSATA cable • 1 x QIG</p>  <p><small>©2023 Copyright by IEI Integration Corp. All rights reserved.</small></p>

Table 2-1: Packing List

HYPER-EHL

2.4 Optional Items

The following are optional components which may be separately purchased:

Item and Part Number	Image
Dual-port USB cable with bracket, 300mm, p=2.0 (P/N: CB-USB02A-RS)	
SATA power cable, MOLEX 5264-4P to SATA15P (P/N: 32102-000100-200-RS)	
PCIe x4 to two PCIe x2 riser card for HYPER on the left side (P/N: HPR-L2S-R10)	
PCIe x4 to four PCIe x1 riser card for HYPER on the left side (P/N: HPR-L4S-R10)	
PCIe x4 to two PCIe x2 riser card for HYPER on the right side (P/N: HPR-R2S-R10)	
PCIe x4 to four PCIe x1 riser card for HYPER on the right side (P/N: HPR-R4S-R10)	



Item and Part Number	Image
eDP to eDP converter board (for IEI iDPM slot) (P/N: iDPM-eDP-R10)	 A green printed circuit board (PCB) with a large black integrated circuit (IC) in the center. It features a gold-plated edge connector on the right side and various surface components like capacitors and resistors.
eDP to LVDS converter board (for IEI iDPM slot) (P/N: iDPM-LVDS-R10)	 A green PCB with a large black IC in the center. It has a gold-plated edge connector on the right and a multi-pin connector on the left. The board is populated with various electronic components.

Table 2-2: Optional Items

Chapter

3

Connectors

3.1 Peripheral Interface Connectors

This chapter details all the peripheral interface connectors.

3.1.1 HYPER-EHL Layout

The figures below show all the peripheral interface connectors.

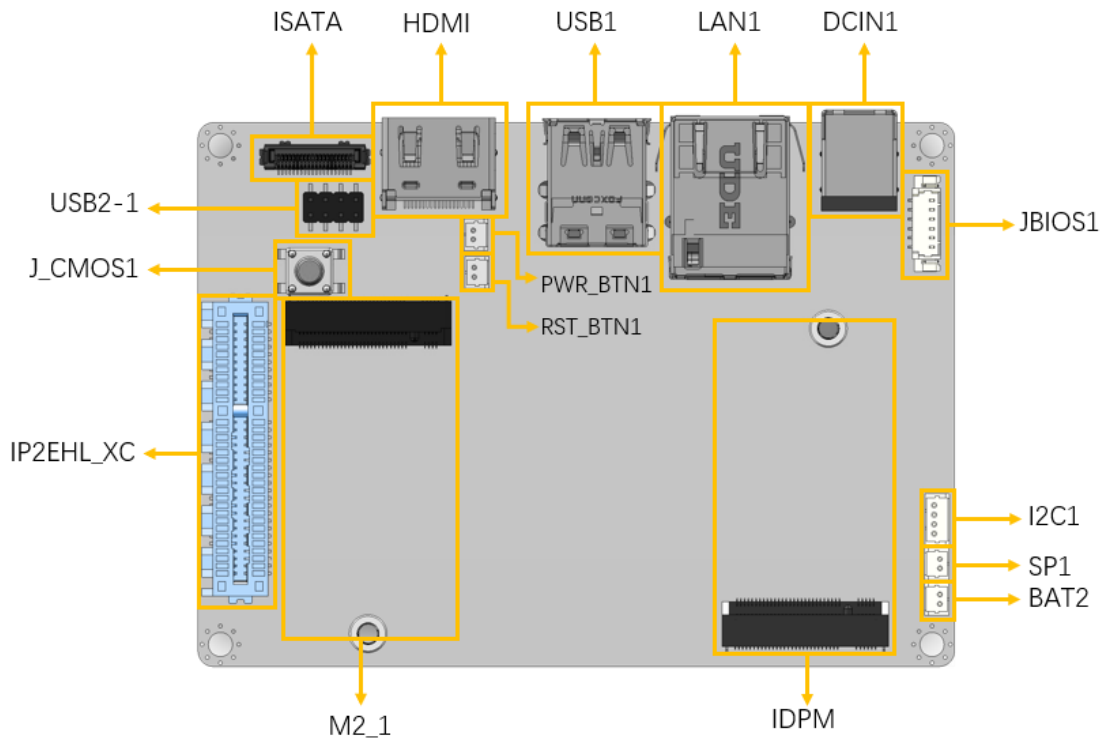


Figure 3-1: Peripheral Interface Connectors

3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
Clear CMOS Button	Button	J_CMOS1
AT/ATX Power Mode Setting Switch	3-pin switch	J_ATX_AT1
Battery Connector	2-pin wafer	BAT2

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Connector	Type	Label
Buzzer Connector	2-pin wafer	SP1
Digital I/O Connector	10-pin wafer	DIO1
Flash SPI ROM Connector	6-pin wafer	JBIOS1
I2C Connector	4-pin wafer	I2C1
iSATA 6Gb/s Connector	20-pin SATA connector	ISATA
Power Button Connector	2-pin header	PWR_BTN1
Reset Button Connector	2-pin header	RST_BTN1
RS-232/422/485 Serial Port Connector	9-pin header	COM1
Internal USB 2.0 Connector	8-pin header	USB2-1
M.2 M-key Slot	M.2 M-key slot	M2_1
PCIe Gen3 x4 Slot	PCIe x4 slot	IP2EHL_XC
IEI iDPM Slot	Button	IDPM

Table 3-1: Peripheral Interface Connectors

3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
External 12V DC Input Jack	Power jack	DCIN1
External 2.5GbE Connector	RJ45	LAN1
External HDMI Connector	HDMI	HDMI1
External Dual USB 10Gb/s Connector	USB 3.2	USB1

Table 3-2: Rear Panel Connectors

3.2 Internal Peripheral Connectors

The section describes all of the connectors on the HYPER-EHL.

3.2.1 Battery Connector



CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.



NOTE:

It is recommended to attach the RTC battery onto the system chassis in which the HYPER-EHL is installed.

CN Label:	BAT2
CN Type:	2-pin wafer
CN Location:	See Figure 3-2
CN Pinouts:	See Table 3-3

A system battery is placed in the battery holder. The battery provides power to the system clock to retain the time when power is turned off.

HYPER-EHL

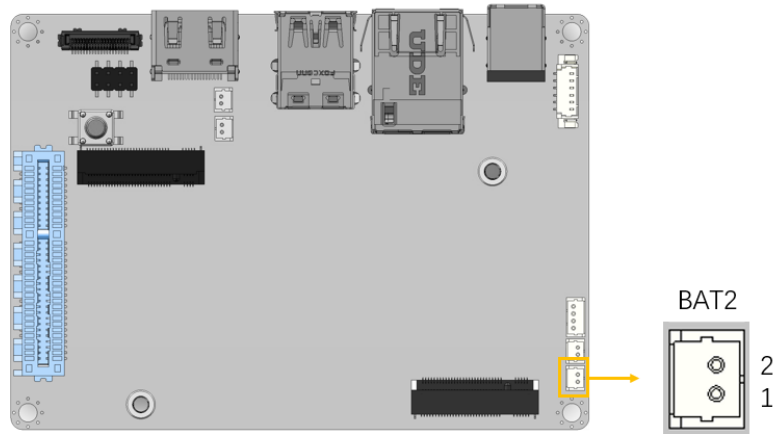


Figure 3-2: Battery Connector Location

Pin	Description	Pin	Description
1	VBATT	2	GND

Table 3-3: Battery Connector Pinouts

3.2.2 AT/ATX Power Mode Setting

- CN Label:** J_ATX_AT1
- CN Type:** 3-pin switch
- CN Location:** See **Figure 3-3**
- CN Pinouts:** See **Table 3-4**

The AT/ATX power mode selection is made through the AT/ATX power mode switch.

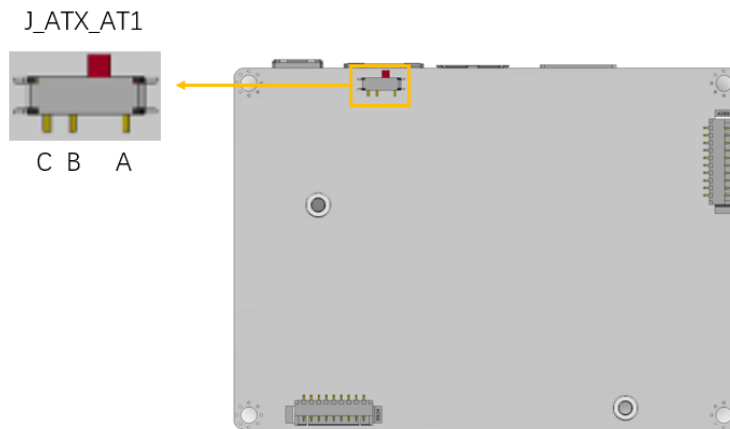


Figure 3-3: AT/ATX Power Mode Switch Location

Pin	Description	Pin	Description
Short A - B	ATX Power Mode (default)	Short B - C	AT Power Mode

Table 3-4: AT/ATX Power Mode Switch Settings

HYPER-EHL

3.2.3 Digital I/O Connector

- CN Label:** DIO1
- CN Type:** 10-pin wafer, p=2.0 mm
- CN Location:** See **Figure 3-4**
- CN Pinouts:** See **Table 3-5**

The Digital I/O connector provides programmable input and output for external devices.

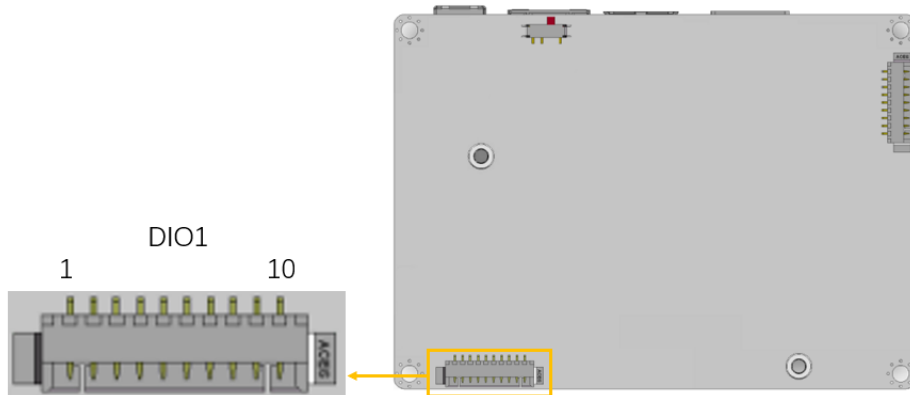


Figure 3-4: Digital I/O Connector Location

Pin	Description	Pin	Description
1	+5V	6	DOUT0
2	DIN0	7	DOUT1
3	DIN1	8	DOUT2
4	DIN2	9	DOUT3
5	DIN3	10	GND

Table 3-5: Digital I/O Connector Pinouts

3.2.4 Clear CMOS Button

- CN Label:** J_CMOS1
- CN Type:** Button
- CN Location:** See **Figure 3-5**
- CN Pinouts:** See **Table 3-6**

The J_CMOS1 is used to Clear CMOS Setup.

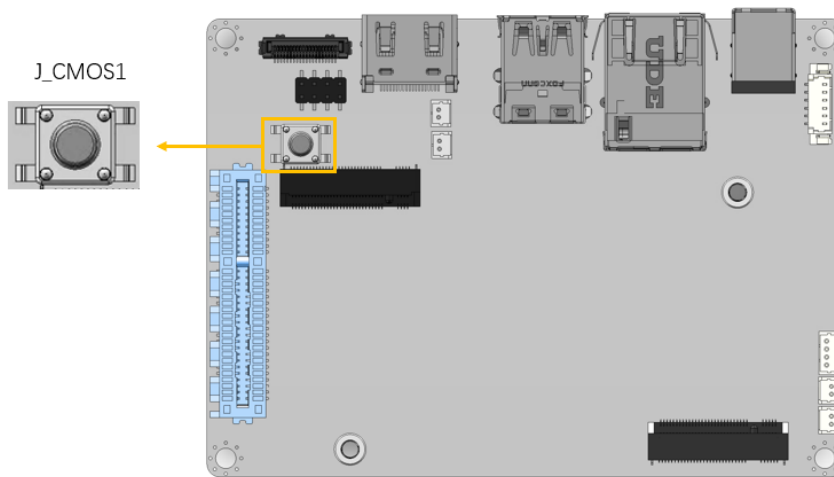


Figure 3-5: Clear CMOS Jumper Location

Pin	Description
NC	Keep CMOS Setup (Normal Operation)
Press	Clear CMOS Setup

Table 3-6: Clear CMOS Jumper Pinouts

HYPER-EHL

3.2.5 I²C Connector

- CN Label:** I2C1
- CN Type:** 4-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-6**
- CN Pinouts:** See **Table 3-7**

The I²C connector is used to connect I²C-bus devices to the mainboard.

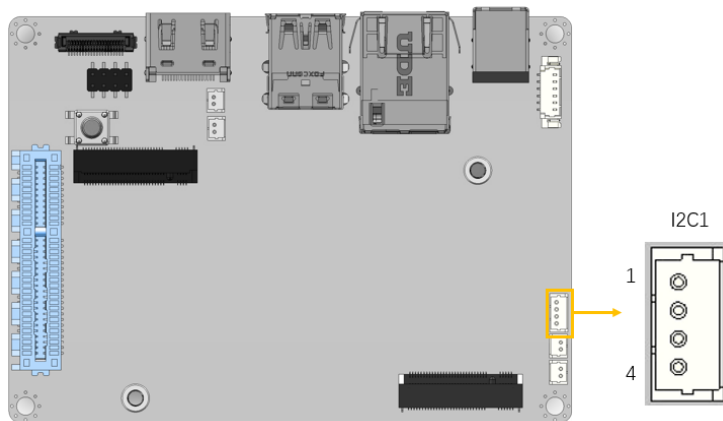


Figure 3-6: I²C Connector Location

Pin	Description	Pin	Description
1	GND	3	I2C_CLK
2	I2C_DATA	4	+5V

Table 3-7: I²C Connector Pinouts

3.2.6 Internal USB 2.0 Connectors

- CN Label:** USB2-1
- CN Type:** 8-pin header, p=2.54 mm
- CN Location:** See Figure 3-7
- CN Pinouts:** See Table 3-8

The Internal USB 2.0 connectors connect to USB 2.0 devices.

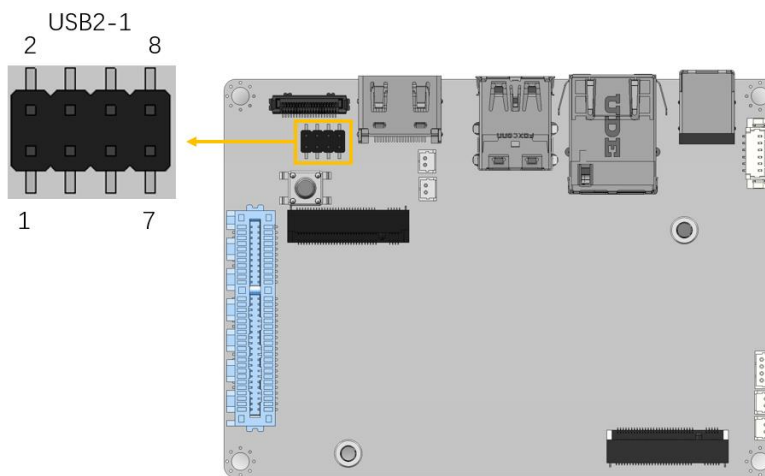


Figure 3-7: Internal USB 2.0 Connector Location

Pin	Description	Pin	Description
1	VCC	2	GND
3	USB_DATA-	4	USB_DATA+
5	USB_DATA+	6	USB_DATA-
7	GND	8	VCC

Table 3-8: Internal USB 2.0 Connector Pinouts

HYPER-EHL

3.2.7 M.2 M-key Slot

- CN Label:** M2_1
- CN Type:** M.2 M-key slot
- CN Location:** See Figure 3-8
- CN Pinouts:** See Table 3-9

The M.2 2242 slot is keyed in the M position.

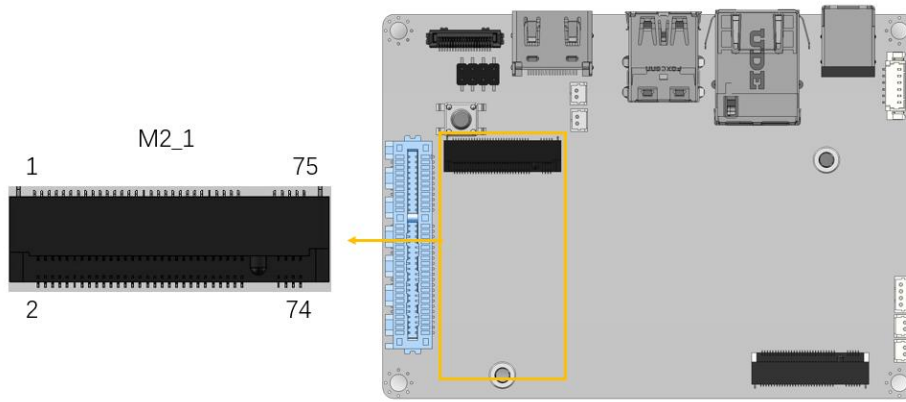


Figure 3-8: M.2 M-key Slot Location

Pin	Description	Pin	Description
1	GND	2	+V3.3A
3	GND	4	+V3.3A
5	NC	6	NC
7	NC	8	NC
9	GND	10	+V3.3A
11	NC	12	+V3.3A
13	NC	14	+V3.3A
15	GND	16	+V3.3A
17	NC	18	+V3.3A
19	NC	20	NC
21	GND	22	NC
23	NC	24	NC
25	NC	26	NC

Pin	Description	Pin	Description
27	GND	28	NC
29	PCIE_RX7-	30	NC
31	PCIE_RX7+	32	NC
33	GND	34	USB+
35	PCIE_TX7-	36	USB-
37	PCIE_TX7+	38	MKEY_SSD_SLP
39	GND	40	M2_I2C_CLK
41	PCIE_RX6-	42	M2_I2C_DATA
43	PCIE_RX6+	44	NC
45	GND	46	NC
47	PCIE_TX6-	48	NC
49	PCIE_TX6+	50	BUF_PLT_RST
51	GND	52	NC
53	CLK_M2_B-	54	PCIE_WAKE#
55	CLK_M2_B+	56	NC
57	GND	58	NC
59	Module Key	60	Module Key
61	Module Key	62	Module Key
63	Module Key	64	Module Key
65	Module Key	66	Module Key
67	NC	68	NC
69	+V3.3A	70	+V3.3A
71	GND	72	+V3.3A
73	GND	74	+V3.3A
75	GND		

Table 3-9: M.2 M-key Connector Pinouts

HYPER-EHL

3.2.8 IEI iDPM Slot

- CN Label:** IDPM
- CN Type:** IDPM slot
- CN Location:** See **Figure 3-9**
- CN Pinouts:** See **Table 3-10**

The iDPM slot is only for IEI eDP/LVDS/VGA module

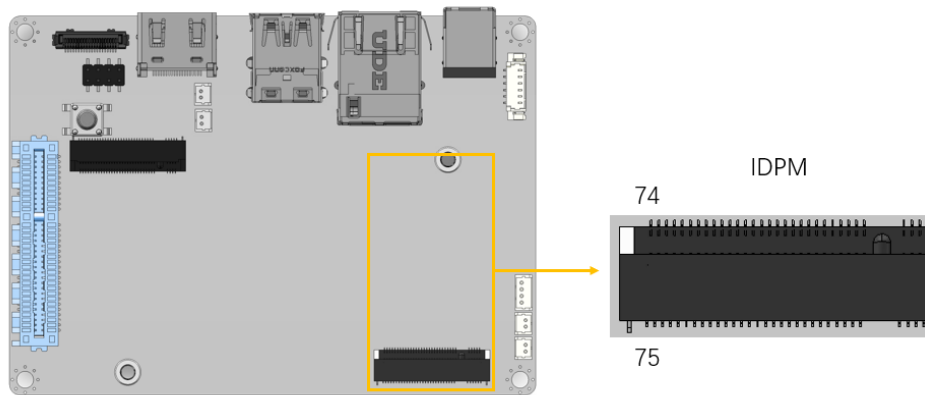


Figure 3-9: iDPM Slot Location

Pin	Description	Pin	Description
1	GND	2	+3.3V
3	GND	4	+3.3V
5	N/C	6	N/C
7	N/C	8	N/C
9	GND	10	NGFF2_ACT_N
11	N/C	12	+3.3V
13	N/C	14	+3.3V
15	GND	16	+3.3V
17	N/C	18	+3.3V
19	N/C	20	N/C
21	GND	22	N/C
23	N/C	24	N/C
25	N/C	26	N/C

Pin	Description	Pin	Description
27	GND	28	N/C
29	PCIE_18_RX_DN	30	N/C
31	PCIE_18_RX_DP	32	N/C
33	GND	34	N/C
35	PCIE_18_TX_DN18	36	N/C
37	PCIE_18_TX_DP18	38	M_2_SATA_SLP
39	GND	40	N/C
41	PCIE_17_RX_DN	42	N/C
43	PCIE_17_RX_DP	44	N/C
45	GND	46	N/C
47	PCIE_17_TX_DN17	48	N/C
49	PCIE_17_TX_DP17	50	PERST_N
51	GND	52	SRCLKREQB_15_N
53	PCIE_SRC15_DN	54	NC
55	PCIE_SRC15_DP	56	N/C
57	GND	58	N/C
59	N/C	60	N/C
61	N/C	62	N/C
63	N/C	64	N/C
65	N/C	66	N/C
67	N/C	68	NC
69	N/C	70	+3.3V
71	GND	72	+3.3V
73	GND	74	+3.3V
75	GND		

Table 3-10: iDPM Connector Pinouts

HYPER-EHL

3.2.9 PCIe x4 Slot

CN Label:	IP2EHL_XC
CN Type:	PCIe x4 slot
CN Location:	See Figure 3-10

The PCIe x4 expansion card slots are for PCIe x4 expansion cards.

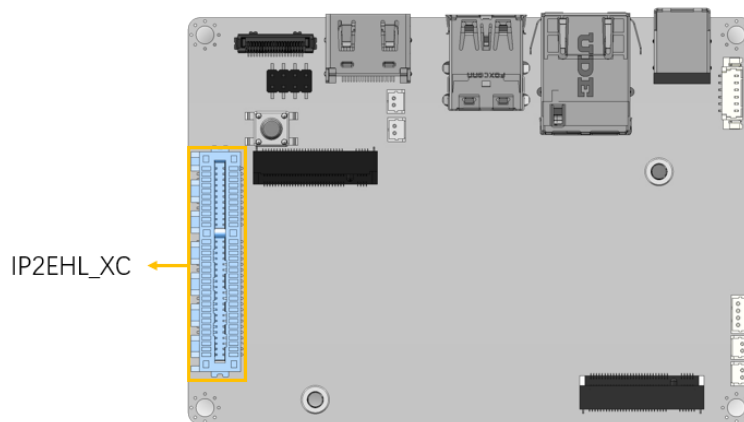


Figure 3-10: PCIe x4 Slot Location

3.2.10 Power Button Connector

CN Label:	PWR_BTN1
CN Type:	2-pin wafer, p=2.00 mm
CN Location:	See Figure 3-11

The power button connector is connected to a power switch on the system chassis to enable users to turn the system on and off.

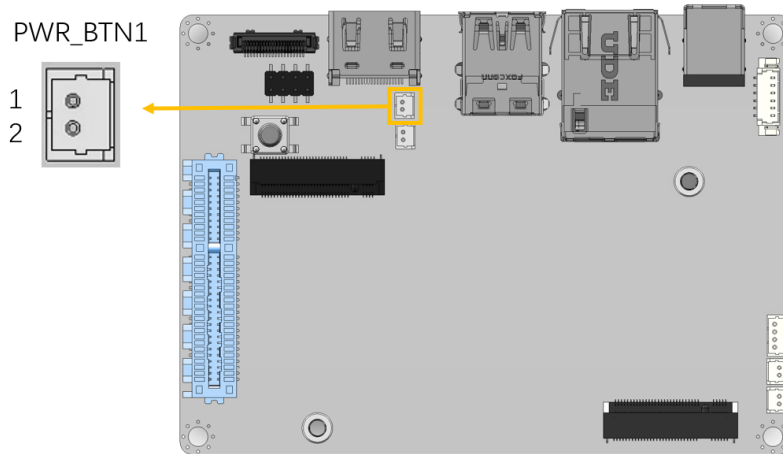


Figure 3-11: Power Button Connector Location

3.2.11 Reset Button Connector

- CN Label:** RST_BTN1
- CN Type:** 2-pin wafer, p=2.00 mm
- CN Location:** See **Figure 3-12**

The reset button connector is connected to a reset switch on the system chassis allows users to reboot the system when the system is turned on.

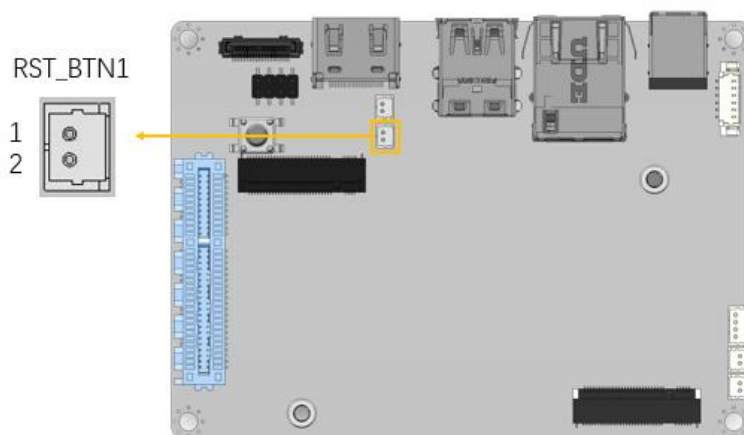


Figure 3-12: Reset Button Connector Location

HYPER-EHL

3.2.12 iSATA 6Gb/s Connectors

- CN Label:** ISATA
- CN Type:** 20-pin SATA connector
- CN Location:** See **Figure 3-13**
- CN Pinouts:** See **Table 3-11**

The iSATA drive connector is connected to a SATA device via a cable defined by IEI. The iSATA drive transfers data at speeds as high as 6Gb/s.

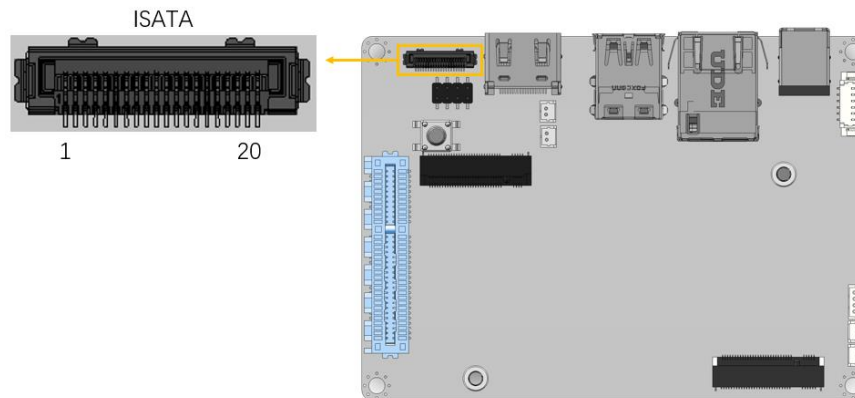


Figure 3-13: iSATA Connector Location

Pin	Description	Pin	Description
1	GND	11	+5V
2	GND	12	N/C
3	GND	13	N/C
4	GND	14	GND
5	GND	15	SATA RX+
6	GND	16	SATA_RX-
7	+5V	17	GND
8	+5V	18	SATA_TX-
9	+5V	19	SATA_TX+
10	+5V	20	GND

Table 3-11: iSATA Connector Pinouts

3.2.13 RS-232/422/485 Serial Port Connector

- CN Label:** COM1
- CN Type:** 9-pin header, p=2.54 mm
- CN Location:** See **Figure 3-14**
- CN Pinouts:** See **Table 3-12**

Each of these connectors provides RS-232/422/485 communications.

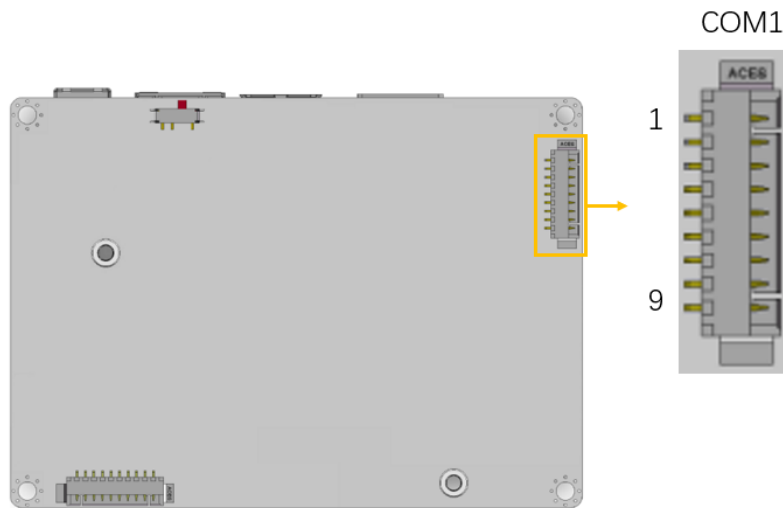


Figure 3-14: RS-232/422/485 Connector Location

Pin	Description	Pin	Description
1	DCD	6	CTS
2	DSR	7	DTR
3	SIN	8	RI
4	RTS	9	GND
5	SOUT		

Table 3-12: RS-232/422/485 Connector Pinouts

HYPER-EHL

3.2.14 Buzzer Connector

- CN Label:** SP1
- CN Type:** 2-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-15**
- CN Pinouts:** See **Table 3-13**

The buzzer connector is connected with the buzzer to give a beep warning when the motherboard goes wrong.

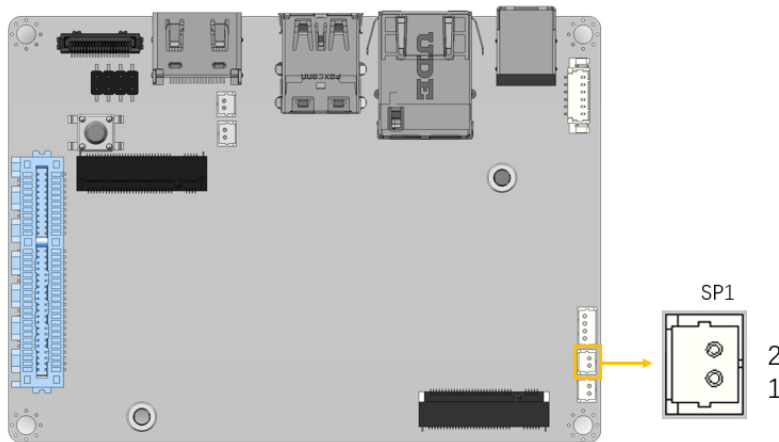


Figure 3-15: Buzzer Connector Location

Pin	Description	Pin	Description
1	+5V	2	PC_BEEP

Table 3-13: Buzzer Connector Pinouts

3.2.15 Flash SPI ROM Connector

- CN Label:** JBIOS1
- CN Type:** 6-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-16**
- CN Pinouts:** See **Table 3-14**

The Flash SPI ROM connector is used to flash the BIOS.

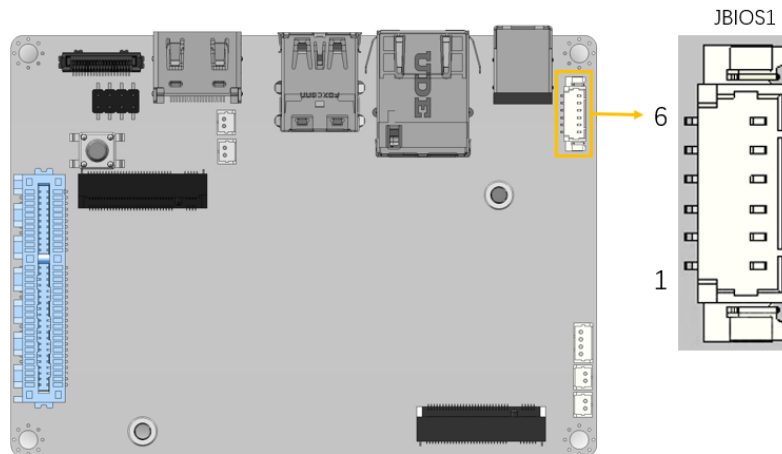


Figure 3-16: Flash SPI ROM Connector Location

Pin	Description	Pin	Description
1	+3.3V	4	SPI_CLK
2	SPI_CS#	5	SPI_SI
3	SPI_SO	6	GND

Table 3-14: Flash SPI ROM Connector Pinouts

HYPER-EHL

3.3 External Peripheral Interface Connector Panel

The figure below shows the external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

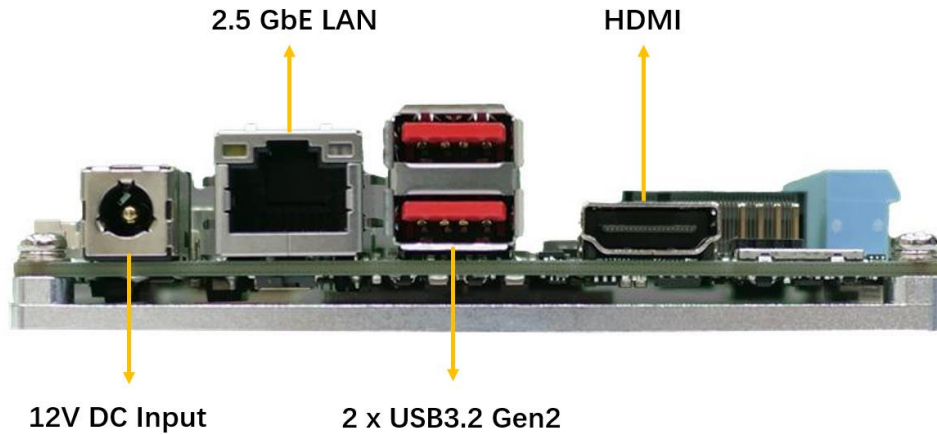


Figure 3-17: External Peripheral Interface Connector

3.3.1 External 12V DC Input Jack

- CN Label:** DCIN1
- CN Type:** Power jack
- CN Location:** See Figure 3-18
- CN Pinouts:** See Table 3-15

The connector supports the 12V power adapter.



Figure 3-18: External 12V DC Input Jack Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	+12V	3	GND
2	GND		

Table 3-15: External 12V DC Input Jack Pinouts

3.3.2 External 2.5GbE RJ-45 Connector

- CN Label:** LAN1
- CN Type:** RJ45
- CN Location:** See Figure 3-19
- CN Pinouts:** See Table 3-16

The LAN connector connects to a local network.

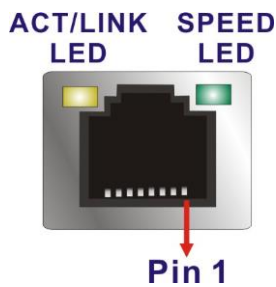


Figure 3-19: LAN Connector

PIN	DESCRIPTION	PIN	DESCRIPTION
1	LAN1_MDI0P	5	LAN1_MDI2P
2	LAN1_MDI0N	6	LAN1_MDI2N
3	LAN1_MDI1P	7	LAN1_MDI3P
4	LAN1_MDI1N	8	LAN1_MDI3N

Table 3-16: 2.5GbE RJ-45 Connector Pinouts

LED	Description	LED	Description
Off	No link	Off	10 Mbps connection
Yellow	Linked	orange	1000 Mbps connection
Blinking	TX/RX activity	Green	2.5 Gbps connection

Table 3-17: LAN LED Pinouts

HYPER-EHL

3.3.3 External HDMI Combo Connector

- CN Label:** HDMI
- CN Type:** HDMI
- CN Location:** See **Figure 3-20**
- CN Pinouts:** See **Table 3-18**

The external HDMI connector can connect to an HDMI device.

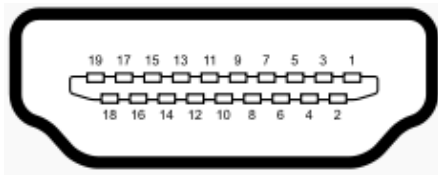


Figure 3-20: External HDMI Connector Location

Pin	Description	Pin	Description
1	HDMI2_DATA2	2	GND
3	HDMI2_DATA2#	4	HDMI2_DATA1
5	GND	6	HDMI2_DATA1#
7	HDMI2_DATA0	8	GND
9	HDMI2_DATA0#	10	HDMI2_CLK
11	GND	12	HDMI2_CLK#
13	N/C	14	N/C
15	HDMI2_SCL	16	HDM2I_SDA
17	GND	18	+5V
19	HDMI2_HPD		

Table 3-18: External HDMI Connector Pinouts

3.3.4 External Dual USB 3.2 Gen2 10Gb/s Connector

- CN Label:** USB1
- CN Type:** USB 3.2
- CN Location:** See Figure 3-21
- CN Pinouts:** See Table 3-19

The external dual USB 3.2 Gen 2 connector can be connected to USB2.0 or USB 3,2 devices.

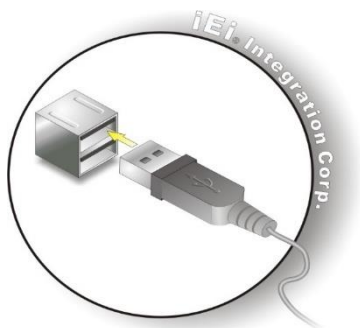


Figure 3-21: External dual USB 3.2 Gen2 Connectors Location

Pin	Description	Pin	Description
1	VCC	10	VCC
2	USB_DATA-	11	USB_DATA-
3	USB_DATA+	12	USB_DATA+
4	GND	13	GND
5	USB3_RX-	14	USB3_RX-
6	USB3_RX+	15	USB3_RX+
7	GND	16	GND
8	USB3_TX-	17	USB3_TX-
9	USB3_TX+	18	USB3_TX+

Table 3-19: External dual USB 3.2 Gen2 Connectors Pinouts

Chapter

4

Installation

4.1 Anti-static Precautions



WARNING:

Failure to take ESD precautions during the installation of the HYPER-EHL may result in permanent damage to the HYPER-EHL and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the HYPER-EHL. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the HYPER-EHL or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- **Wear an anti-static wristband:** Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- **Self-grounding:** Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- **Use an anti-static pad:** When configuring the HYPER-EHL, place it on an anti-static pad. This reduces the possibility of ESD damaging the HYPER-EHL.
- **Only handle the edges of the PCB:** When handling the PCB, hold the PCB by the edges.

4.2 Installation Considerations



NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

HYPER-EHL



WARNING:

The installation instructions described in this manual should be carefully followed in order to prevent damage to the components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
 - The user manual provides a complete description of the HYPER-EHL installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
 - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the HYPER-EHL on an anti-static pad:
 - When installing or configuring the motherboard, place it on an anti-static pad. This helps to prevent potential ESD damage.
- Turn all power to the HYPER-EHL off:
 - When working with the HYPER-EHL, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the HYPER-EHL, **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.3 M.2 Module Installation

The HYPER-EHL provide two ways to install the M.2 expansion card. One is using screw, and the other is using the retainer. Please follow the steps below.

Mode One: Using screw

- Step 1:** Locate the M.2 module slot. See **Chapter 3**.
- Step 2:** Remove the retention screw secured on the motherboard.
- Step 3:** Line up the notch on the module with the notch on the slot. Slide the M.2 module into the socket at an angle of about 20° (**Figure 4-1**).

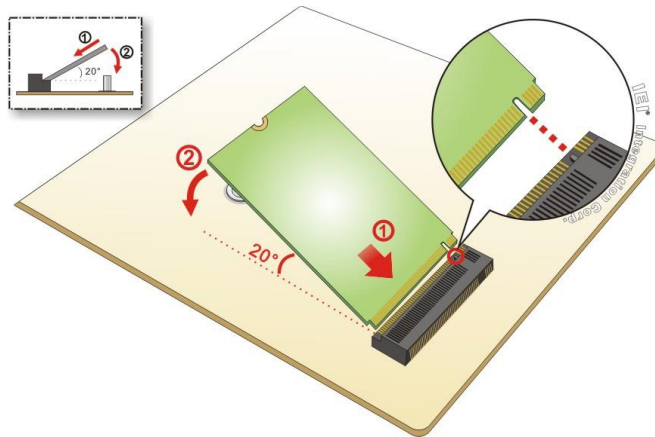


Figure 4-1: Inserting the M.2 Module into the Slot at an Angle

- Step 4:** Secure the M.2 module with the previously removed retention screw (**Figure 4-2**).

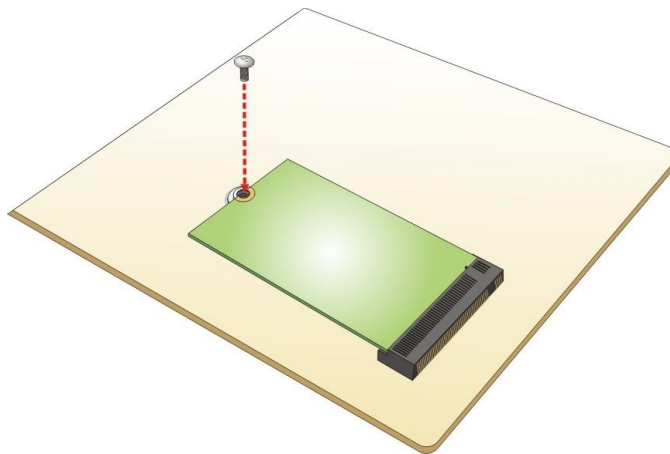


Figure 4-2: Securing the M.2 Module

HYPER-EHL

Mode Two: Using the Retainer

Step 1: Press the retainer down as shown below. (See **Figure 4-3**)

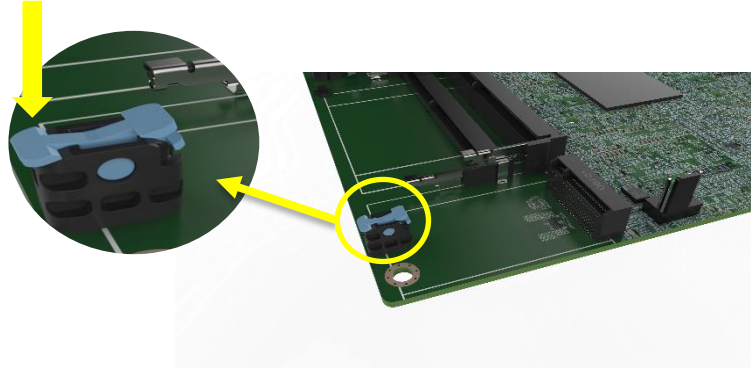


Figure 4-3: Press the Retainer

Step 2: Line up the notch on the M.2 module with the notch on the slot. Slide the M.2 module into the socket at an angle of about 20°. (See **Figure 4-1**)

Step 3: Align the notch on the end of the M.2 module with the clip of the retainer. (See **Figure 4-4**)

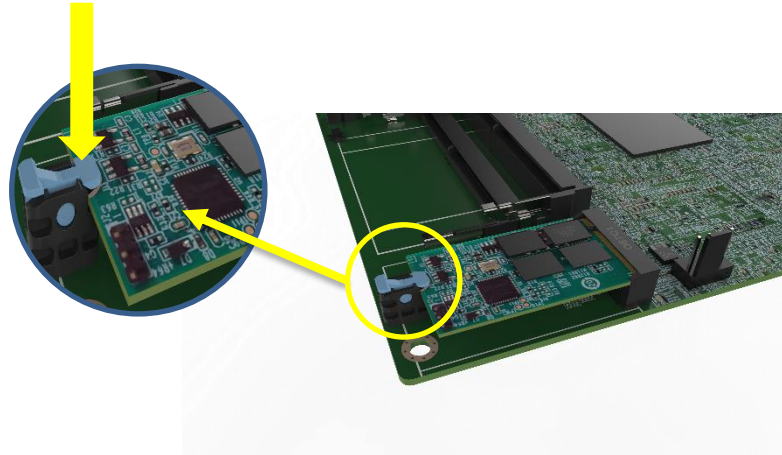


Figure 4-4: Aligning the M.2 Module with the Retainer

Step 4: Press the M.2 module down until it is secured into place by the retainer. (See **Figure 4-5**)

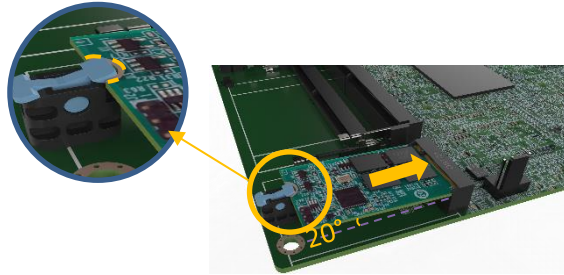


Figure 4-5: Securing the M.2 Module

Step 5: If you want to remove the M.2 module, you should press the retainer down as described in Step 1 to release the M.2 module. (See **Figure 4-3**)

4.4 Riser Card Installation

The HYPER-EHL features a PCIe x4 (x4 signal) slot, which is a new design of the motherboard to expand functionality. By installing an IEI-developed riser card into the PCIe slot, the x4 signal is divided into x4 or x2+x2 or 1+x1+x1+x1 slots, offering great configuration flexibility and expandability.

Four types of riser cards with different orientation are available, two with slots facing outwards and the other with slots facing inwards.

All the riser cards can be firmly secured to enhance stability by using the L-shaped bracket, in which screw holes are perfectly matched with those on the side of the heatsink and on the riser card, making it easy and convenient to install.

HYPER-EHL

4.4.1 The inwards-facing riser card

The inwards-facing riser card (P/N: HPR-R2S-R10, HPR-R4S-R10), although lower in height, is able to provide better spacing to ensure expansion cards to run at a low temperature. It is ideal for the chassis that is wide enough for the expansion card to be placed.

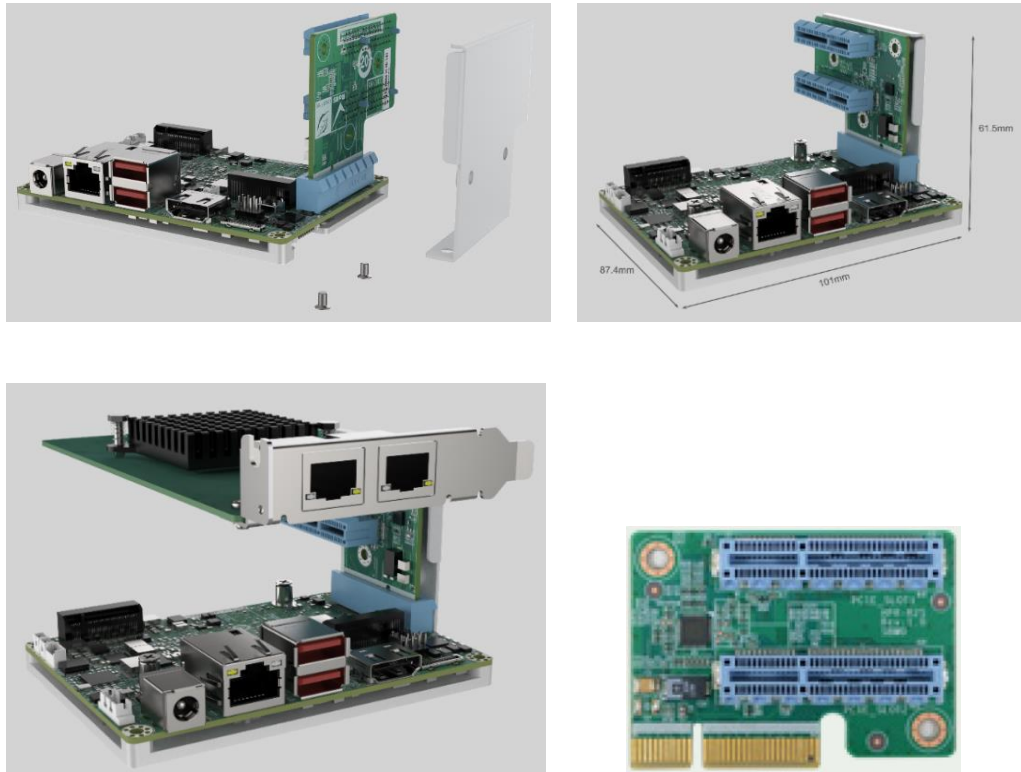
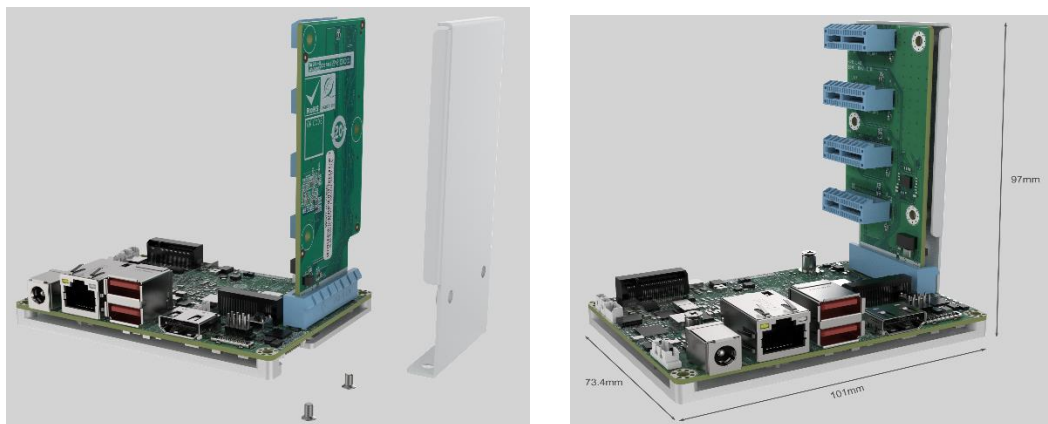


Figure 4-6: Inwards Riser Card Installation Example (P/N: HPR-R2S-R10)



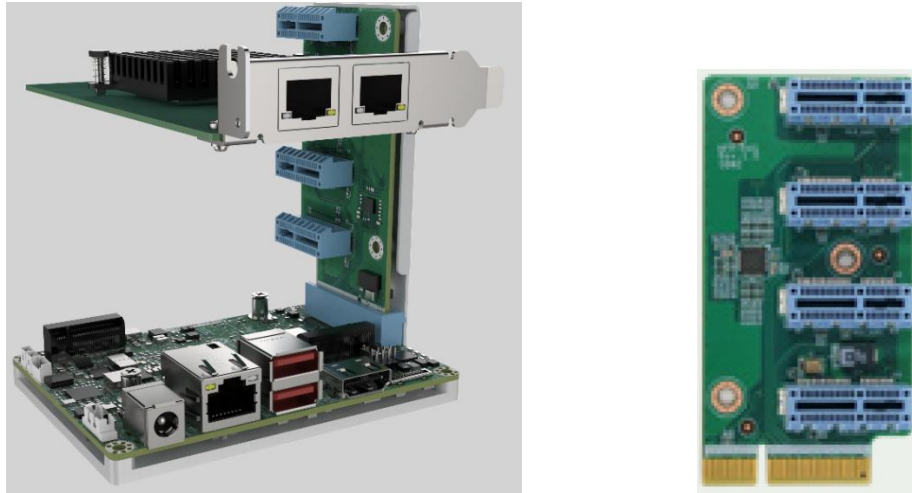


Figure 4-7: Inwards Riser Card Installation Example (P/N: HPR-R4S-R10)

4.4.2 The outwards-facing riser card

The inwards-facing riser card (P/N: NWR-L2S- R10, NWR-L4S- R10) is designed with higher height to keep a decent space between the expansion cards and the motherboard. This can help improve the airflow and heat transfer within the system. It is suitable for installation where space is limited.

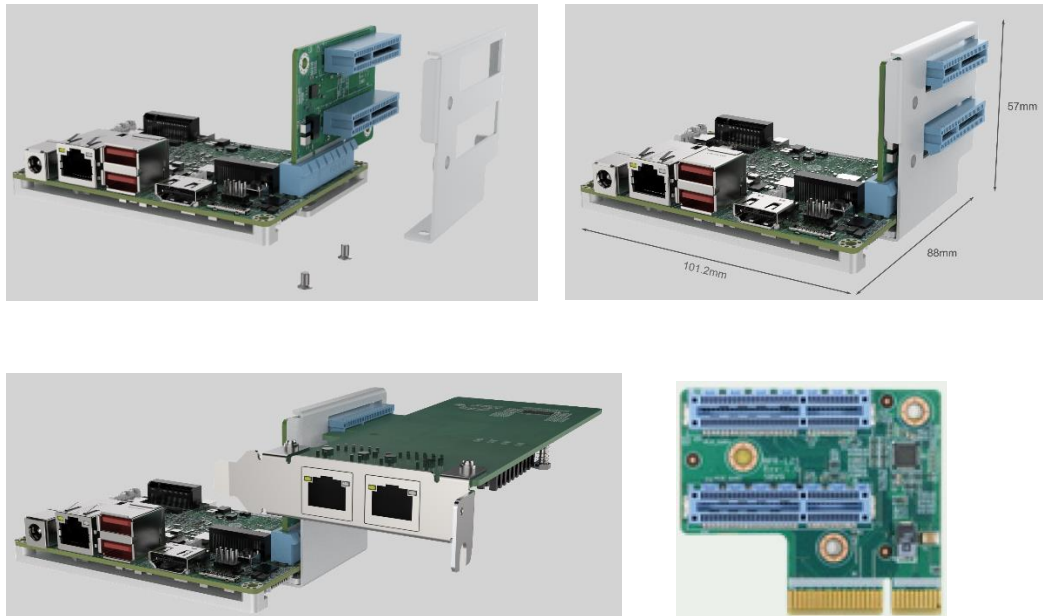


Figure 4-8: Outwards Riser Card Installation Example (P/N: NWR-L2S-R10)

HYPER-EHL

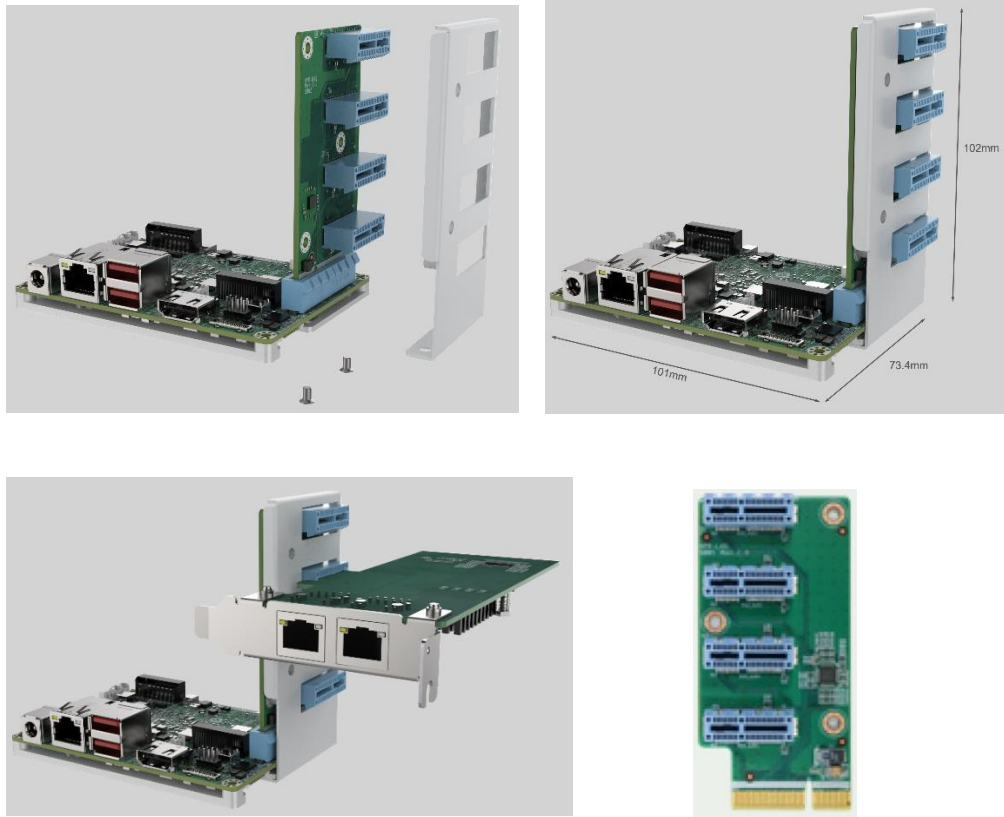


Figure 4-9: Outwards Riser Card Installation Example (P/N: NWR-L4S-R10)

4.5 Software Installation

All the drivers for the HYPER-EHL are available on IEI Resource Download Center (<https://download.ieiworld.com>). Type HYPER-EHL and press Enter to find all the relevant software, utilities, and documentation.

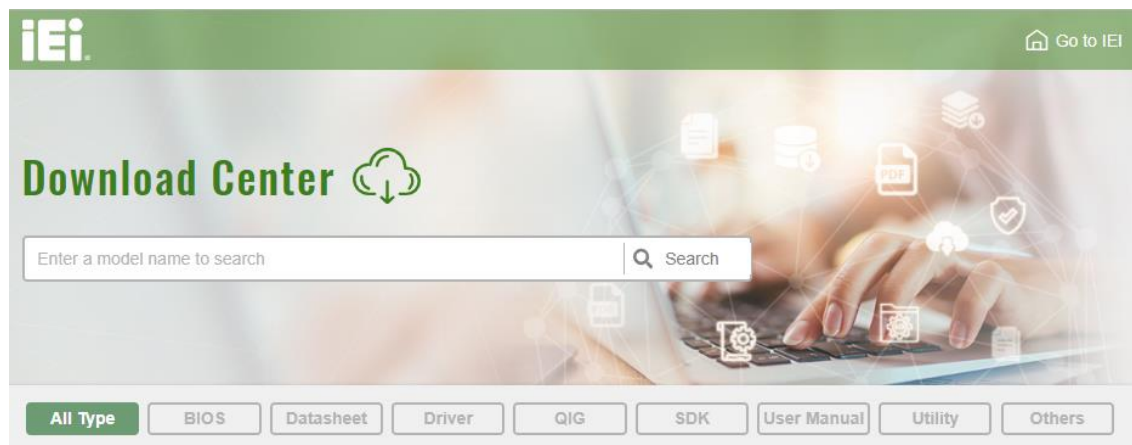
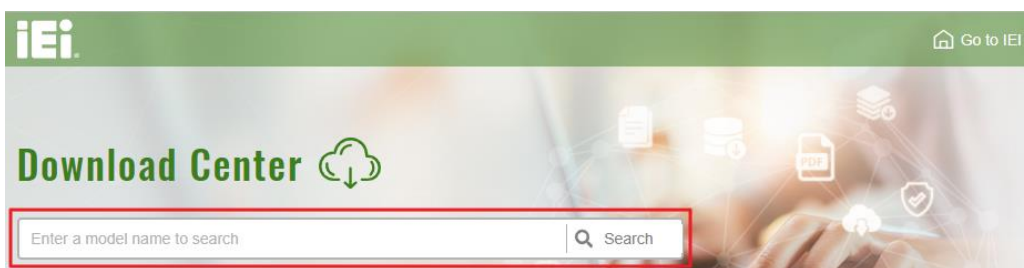


Figure 4-10: IEI Resource Download Center

4.6 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

Step 1: Go to <https://download.ieiworld.com>. Type HYPER-EHL and press Enter.



Step 2: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.


HYPER-EHL

[All Type](#)
[BIOS](#)
[Datasheet](#)
[Driver](#)
[QIG](#)
[SDK](#)
[User Manual](#)
[Utility](#)
[Others](#)

WAFER-BT-i1 [Product Info](#)

[Embedded Computer](#) ▶ [Single Board Computer](#) ▶ [Embedded Board](#)
 3.5" SBC with Intel® 22nm Atom™/Celeron® on-board SoC

Driver

File Name	Published	Version	File Checksum
7B000-001033-RS V2.3.iso (2.23 GB) 	2017/10/03	2.30	3B2DB1F792779A93A8F50DDBC3943E30

Step 3: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or click the small arrow to find an individual driver and click the file name to download (❷).

7B000-001168-RS_V1.4.iso

❶ [Click here to download entire ISO file. \(2.99 GB\)](#)

* Download individual file *

- Docs
 - 1.Chipset
 - ❷ 10.1.1.12.zip (2.7 MB)
 - 2.VGA
 - 3.Audio
 - 4.Lan
 - 5.USB 3.0
 - 6.Serial IO
 - 7.TXE
 - 8.Manual



NOTE:

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content. On Windows 7 system, an additional tool (such as Virtual CD-ROM Control Panel from Microsoft) is needed to mount the file.

Chapter

5

BIOS

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.



NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. **Using keyboard:** Press the **DEL** or **F2** as soon as the system is turned on.
2. **Using touchscreen:** Press the **Setup** button on the upper right corner of the BIOS Starting Menu.

If the message disappears before the **DEL** or **F2** key is pressed, restart the computer and try again, then the BIOS Starting Menu will appear. Select "Setup" and press Enter to get into the BIOS Setup.

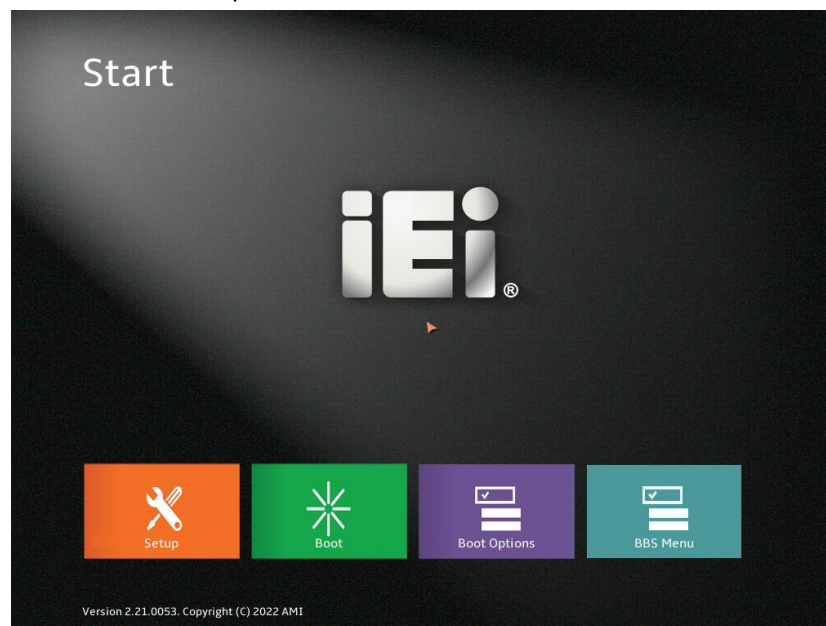


Figure 5-1: BIOS Starting Menu

5.1.2 Using Setup

The BIOS Setup menu can be navigated by using a keyboard or a touchscreen.

5.1.2.1 Keyboard Navigation

For keyboard navigation, use the navigation keys shown in **Table 5-1**.

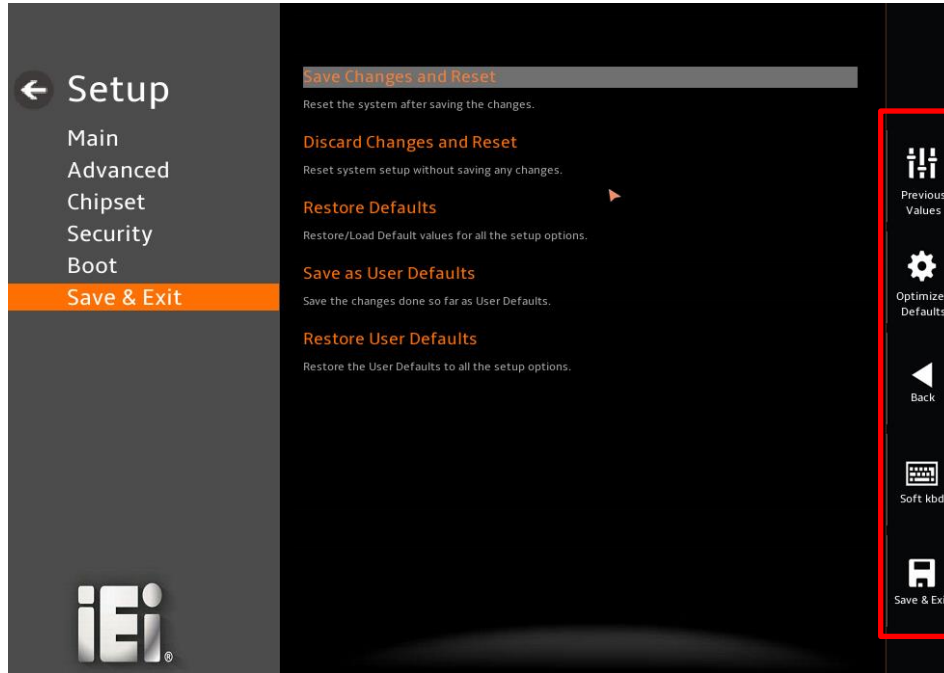
Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes
-	Decrease the numeric value or make changes
Page Up	Move to the previous page
Page Dn	Move to the next page
Esc	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Load previous values
F3	Load optimized defaults
F4	Save changes and Exit BIOS
<K>	Scroll help area upwards
<M>	Scroll help area downwards

Table 5-1: BIOS Navigation Keys

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5.1.2.2 Touch Navigation

For touchscreen navigation, use the on-screen navigation keys shown below.



On-screen Button	Function
Previous Values	Load the last value you set.
Optimized Defaults	Load the factory default values in order to achieve the best performance.
Back	Return to the previous menu.
Soft kbd	Display the on-screen keyboard.
Save & Exit	Save the changes made to the BIOS options and reset the system.

Table 5-2: BIOS On-screen Navigation Keys

5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press the **Esc** key.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the clear CMOS button described in **Chapter 4**.

5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

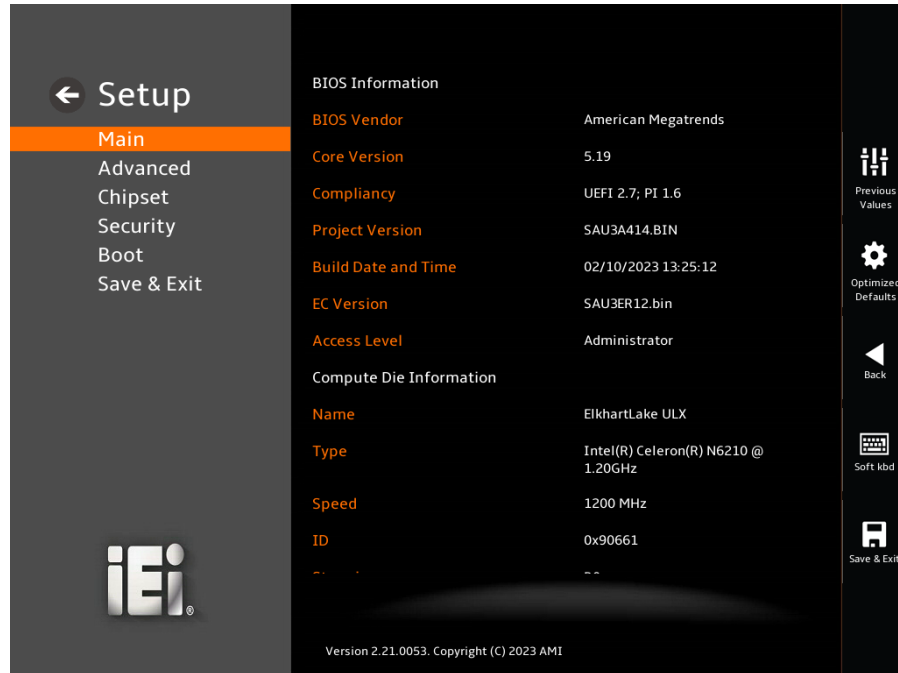
- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

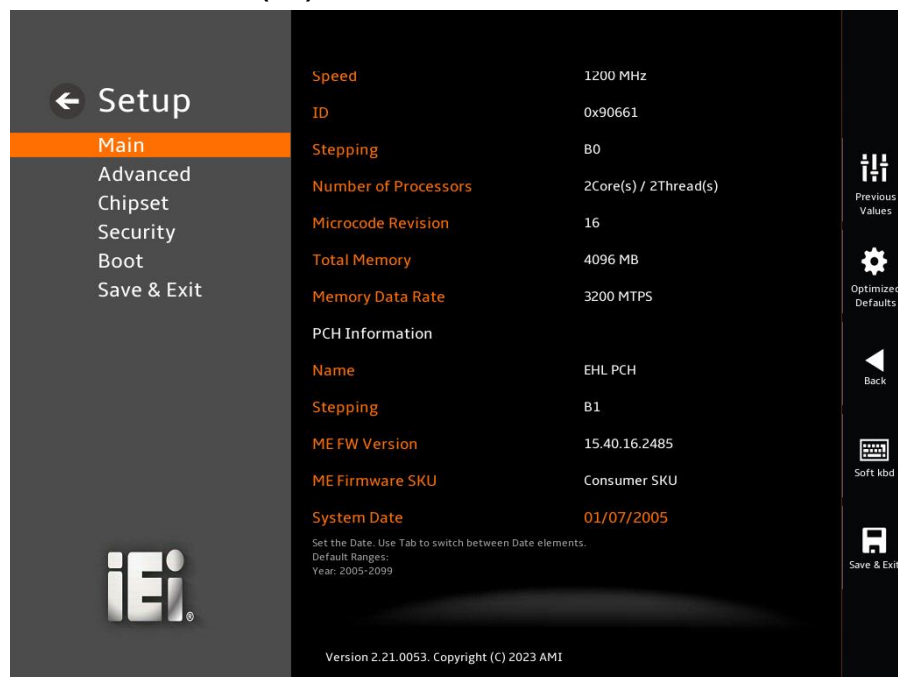
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5.2 Main

The **Main** BIOS menu (**BIOS Menu 2**) appears when the **BIOS Setup** program is entered. The **Main** menu gives an overview of the basic system information.



BIOS Menu 1: Main (1/3)



BIOS Menu 2: Main (2/3)



BIOS Menu 3: Main (3/3)

➔ **BIOS Information**

The **BIOS Information** lists a brief summary of the BIOS. The fields in **BIOS Information** cannot be changed. The items shown in the system overview include:

- **BIOS Vendor:** Installed BIOS vendor
- **Core Version:** Current BIOS version
- **Compliance:** Current UEFI & PI version
- **Project Version:** the board version
- **Build Date and Time:** Date the current BIOS version was made
- **EC Version:** Current EC version

➔ **Processor Information**

The **Processor Information** lists a brief summary of the Processor. The fields in **Processor Information** cannot be changed. The items shown in the system overview include:

- **Name:** Displays the Processor Details
- **Type:** Displays the Processor Type

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- **Speed:** Displays the Processor Speed
- **ID:** Displays the Processor ID

→ PCH Information

The **PCH Information** lists a brief summary of the PCH. The fields in **PCH Information** cannot be changed. The items shown in the system overview include:

- **Name:** Displays the PCH Name
- **PCH SKU:** Displays the PCH SKU
- **Stepping:** Displays the PCH Stepping
- **TXT Capability of Platform/PCH:** Displays the TXT Capability
- **Production Type:** Displays the Production Type
- **ME FW Version:** Displays the ME Firmware Version
- **ME Firmware SKU:** Displays the ME Firmware SKU
- **PMC FW Version:** Displays the PMC Firmware Version

→ System Date [xx/xx/xx]

Use the **System Date** option to set the system date. Manually enter the day, month and year.

→ System Time [xx:xx:xx]

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

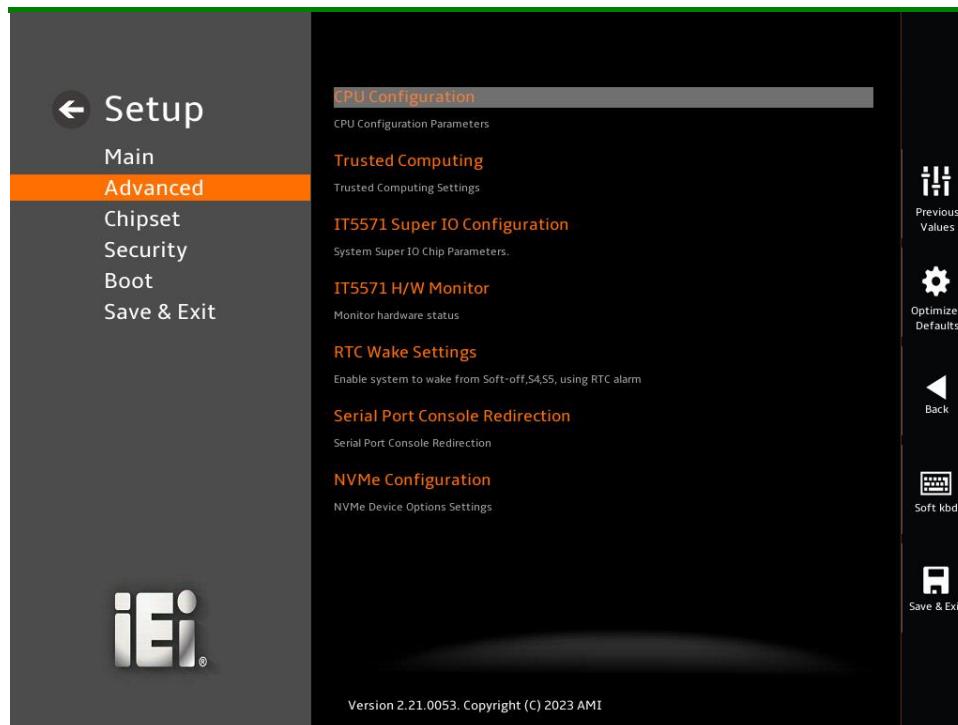
5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 4**) to configure the CPU and peripheral devices through the following sub-menus:



WARNING!

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.



BIOS Menu 4: Advanced

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5.3.1 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 5**) to view detailed CPU specifications or enable the Intel Virtualization Technology.



BIOS Menu 5: CPU Configuration (1/3)

← Setup

- Main
- Advanced**
- Chipset
- Security
- Boot
- Save & Exit

VMX Supported

SMX/TXT Not Supported

Package TDP Limit 6.500

Power Limit 1 6.500

Power Limit 2 20.0

Intel (VMX) Virtualization Technology Enabled

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Active Processor Cores All

Number of cores to enable in each processor package.

Intel(R) SpeedStep(tm) Enabled

Allows more than two frequency ranges to be supported.

C states Disabled

Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.

Tcc Activation Offset 0

Offset from factory set Tcc activation temperature at which the Thermal Control Circuit must be activated. Tcc will be activated at: Tcc Activation Temp - Tcc Activation Offset. Tcc Activation Offset range is 0 to 63.

Previous Values

Optimized Defaults

Back

Soft kbd

Save & Exit

iEi

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BIOS Menu 6: CPU Configuration (2/3)

← Setup

- Main
- Advanced**
- Chipset
- Security
- Boot
- Save & Exit

Allows more than two frequency ranges to be supported.

C states Disabled

Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.

Tcc Activation Offset 0

Offset from factory set Tcc activation temperature at which the Thermal Control Circuit must be activated. Tcc will be activated at: Tcc Activation Temp - Tcc Activation Offset. Tcc Activation Offset range is 0 to 63.

Power Limit 1 0

Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP Limit. If value is 0, BIOS will program TDP value.

Power Limit 1 Time Window 0

Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.

Power Limit 2 0

Power Limit 2 value in Milli Watts; BIOS will round to the nearest 1/8W when programming. If the value is 0, BIOS will program this value as 1.25*TDP. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.

Turbo Mode Enabled

Enable/Disable processor Turbo Mode (requires EMTM enabled too). AUTO means enabled.

Previous Values

Optimized Defaults

Back

Soft kbd

Save & Exit

iEi

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BIOS Menu 7: CPU Configuration (3/3)

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→ Intel (VMX) Virtualization Technology [Enabled]

Use the **Intel (VMX) Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

- **Disabled** Disables Intel Virtualization Technology.
- **Enabled** **DEFAULT** Enables Intel Virtualization Technology.

→ Active Processor Cores [All]

Use the **Active Processor Cores** BIOS option to enable numbers of P-cores in the processor package.

- **All** **DEFAULT** Enable all P-cores in the processor package.
- **1** Enable one P-core in the processor package.

→ Intel(R) SpeedStep(tm) [Enabled]

Use the **Intel(R) SpeedStep(tm)** option to enable or disable the Intel® SpeedStep Technology which allows more than two frequency ranges to be supported.

- **Disabled** Disables Intel® SpeedStep Technology
- **Enabled** **DEFAULT** Enables Intel® SpeedStep Technology

→ C states [Disabled]

Use the **C states** option to enable or disable CPU power management which allows CPU to go to C states when it is not 100% utilized.

- **Disabled** **DEFAULT** Disables CPU power management
- **Enabled** Enables CPU power management

→ Tcc Activation Offset [0]

Use the **Tcc Activation Offset** option to set Tcc activation temperature at which the Thermal Control Circuit must be activated. Tcc will be activated at: Tcc Activation Temp-Tcc Activation Offset. Tcc Activation Offset range is 0 to 63.

→ Power Limit 1 [0]

Use the + or – key to change the **Power Limit 1** value. BIOS will program the default values for Limit 1 and Power Limit 1 Time Window. For 12.50W, enter 12500.

→ Power Limit 1 Time Window [0]

Use the **Power Limit 1 Time Window** option to select the PL1 time duration. The value may vary from 0 to 128. For 0 is the default value

→ Power Limit 2 [0]

Use the + or – key to change the **Power Limit 2** value. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500.

→ Turbo Mode [Enabled]

Use the **Turbo Mode** option to enable or disable Turbo Mode which requires Intel Speed Step or Intel Speed Shift to be available and enabled.

- | | | |
|-------------------|----------------|--------------------------------|
| → Disabled | | Disables Turbo Mode Technology |
| → Enabled | DEFAULT | Enables Turbo Mode Technology |

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5.3.2 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 8**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).



BIOS Menu 8: PCH-FW Configuration

→ Security Device Support [Enable]

Use the **Security Device Support** option to enable or disable BIOS support for security device.

- **Disable** TPM support is disabled.
- **Enable** DEFAULT TPM support is enabled.

→ Pending Operation [None]

Use the **Pending Operation** option to schedule an operation for the security device.

- **None** DEFAULT TPM information is previous.S
- **TPM Clear** TPM information is cleared

5.3.3 IT5571 Super IO Configuration

Use the **IT5571 Super IO Configuration** menu (**BIOS Menu 9**) to set or change the configurations for serial port.

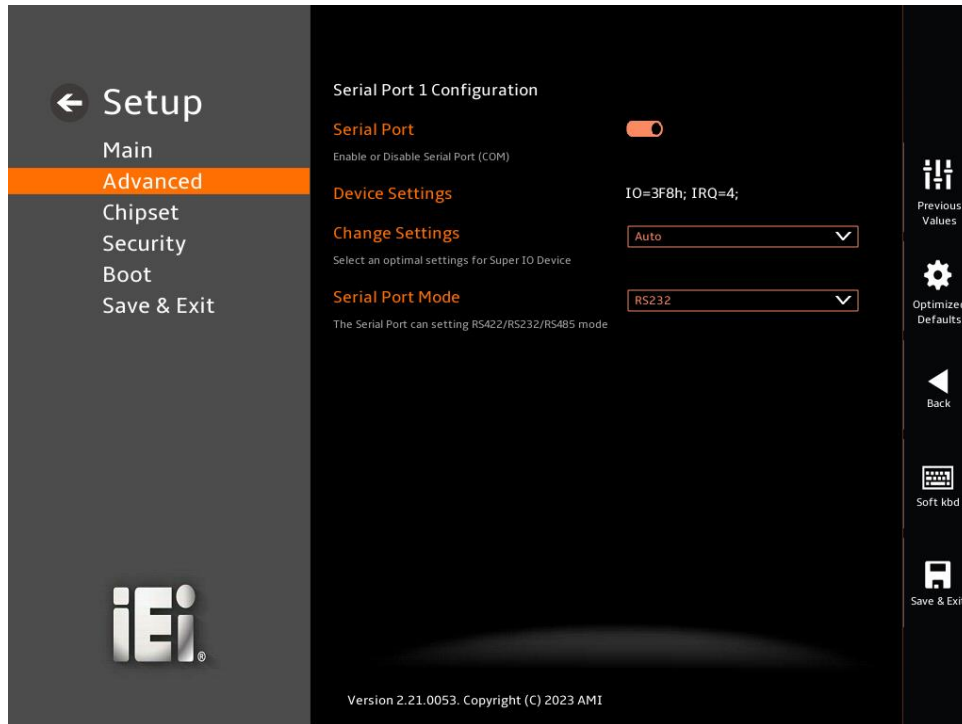


BIOS Menu 9: IT5571 Super IO Configuration

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5.3.3.1 Serial Port 1 Configuration

Use the **Serial Port 1 Configuration** menu (**BIOS Menu 10**) to configure the serial port.



BIOS Menu 10: Serial Port 1 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled** Disable the serial port
- ➔ **Enabled DEFAULT** Enable the serial port

➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

- ➔ **IO=3F8h;** Serial Port I/O port address is 3F8h and the
- IRQ=4** interrupt address is IRQ4

➔ **Device Mode [RS232]**

Use the **Device Mode** option to change the serial port mode.

- ➔ **RS232** **DEFAULT** The serial port mode is RS-232
- RS422 with Register** The serial port mode is RS-422
- RS485 with Register** The serial port mode is RS-485

5.3.4 IT5571 H/W Monitor

The **IT5571 H/W Monitor** menu (**BIOS Menu 11**) contains the smart fan mode configuration submenu and shows the state of H/W real-time operating temperature, fan speeds and system voltages.



BIOS Menu 11: IT5571 H/W Monitor

➔ **PC Health Status**

The following system parameters and values are shown. The system parameters that are monitored are:

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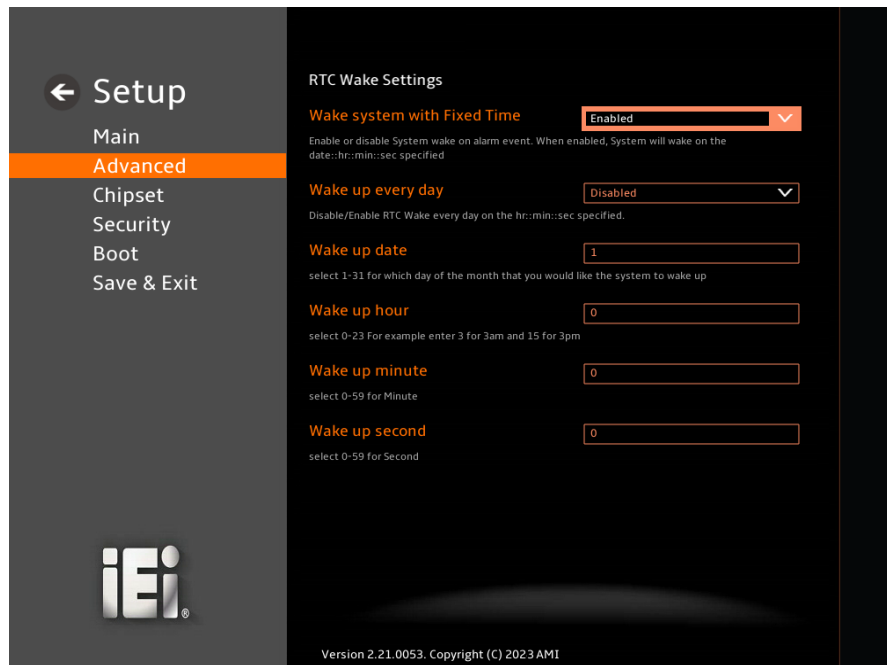
- System Temperatures:
 - CPU Temperature
 - System Temperature
- Voltages:
 - CPU_CORE
 - +5V
 - +12V
 - +DDR
 - +3.3V

5.3.5 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 12**) configures RTC wake event.



BIOS Menu 12: RTC Wake Settings (1/2)



BIOS Menu 13: RTC Wake Settings (2/2)

➔ **Wake system with Fixed Time [Enabled]**

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

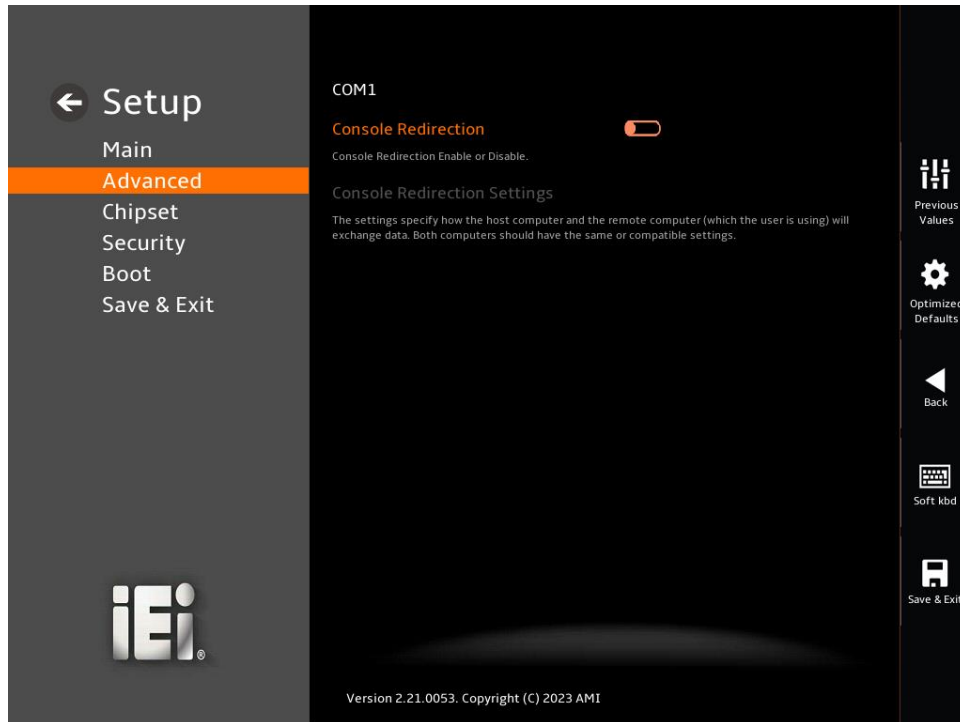
- ➔ **Disabled** The real time clock (RTC) cannot generate a wake event
- ➔ **Enabled DEFAULT** If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be selected:
 - Wake up date
 - Wake up hour
 - Wake up minute
 - Wake up second

After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

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5.3.6 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 14**) allows the console redirection options to be configured. Console Redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



BIOS Menu 14: Serial Port Console Redirection

➔ **Console Redirection [Disabled]**

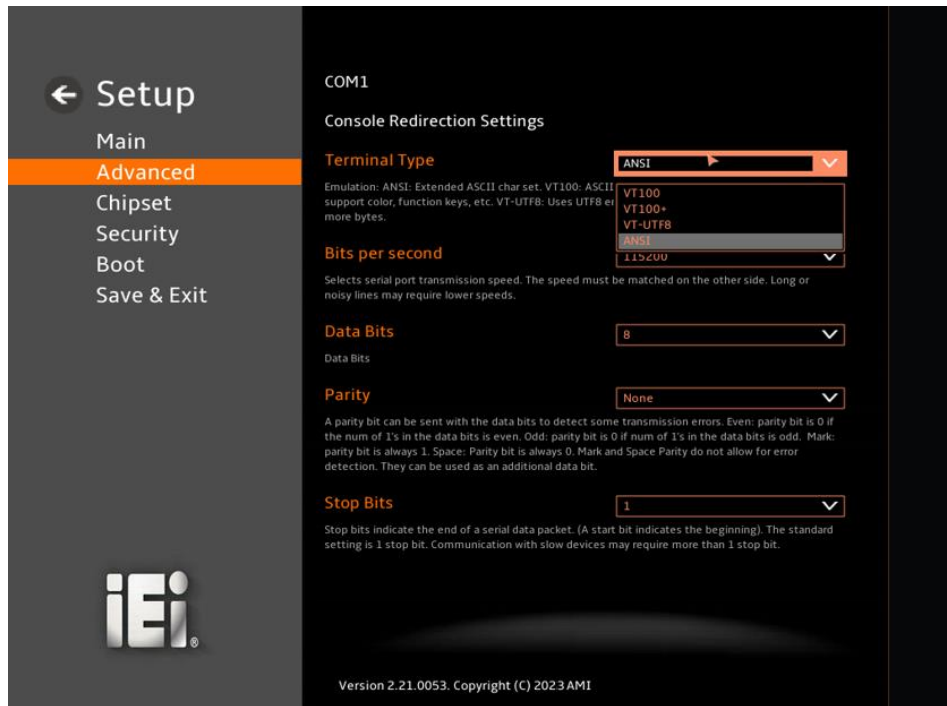
Use **Console Redirection** option to enable or disable the console redirection function.

- ➔ **Disabled** **DEFAULT** Disabled the console redirection function
- ➔ **Enabled** Enabled the console redirection function

The **Console Redirection Settings** submenu will be available when the **Console Redirection** option is enabled.

5.3.6.1 Console Redirection Settings

The following options are available in the **Console Redirection Settings** submenu (**BIOS Menu 15**) when the **COM Console Redirection** (for COM1) option is enabled.



BIOS Menu 15: COM Console Redirection Settings

➔ Terminal Type [ANSI]

Use the **Terminal Type** option to specify the remote terminal type.

- ➔ **VT100** The target terminal type is VT100
- ➔ **VT100+** The target terminal type is VT100+
- ➔ **VT-UTF8** The target terminal type is VT-UTF8
- ➔ **ANSI** **DEFAULT** The target terminal type is ANSI

➔ Bits per second [115200]

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match on the other side. Long or noisy lines may require lower speeds.

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- **9600** Sets the serial port transmission speed at 9600.
- **19200** Sets the serial port transmission speed at 19200.
- **38400** Sets the serial port transmission speed at 38400.
- **57600** Sets the serial port transmission speed at 57600.
- **115200** **DEFAULT** Sets the serial port transmission speed at 115200.

→ Data Bits [8]

Use the **Data Bits** option to specify the number of data bits.

- **7** Sets the data bits at 7.
- **8** **DEFAULT** Sets the data bits at 8.

→ Parity [None]

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

- **None** **DEFAULT** No parity bit is sent with the data bits.
- **Even** The parity bit is 0 if the number of ones in the data bits is even.
- **Odd** The parity bit is 0 if the number of ones in the data bits is odd.
- **Mark** The parity bit is always 1. This option does not allow for error detection.
- **Space** The parity bit is always 0. This option does not allow for error detection.

→ Stop Bits [1]

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

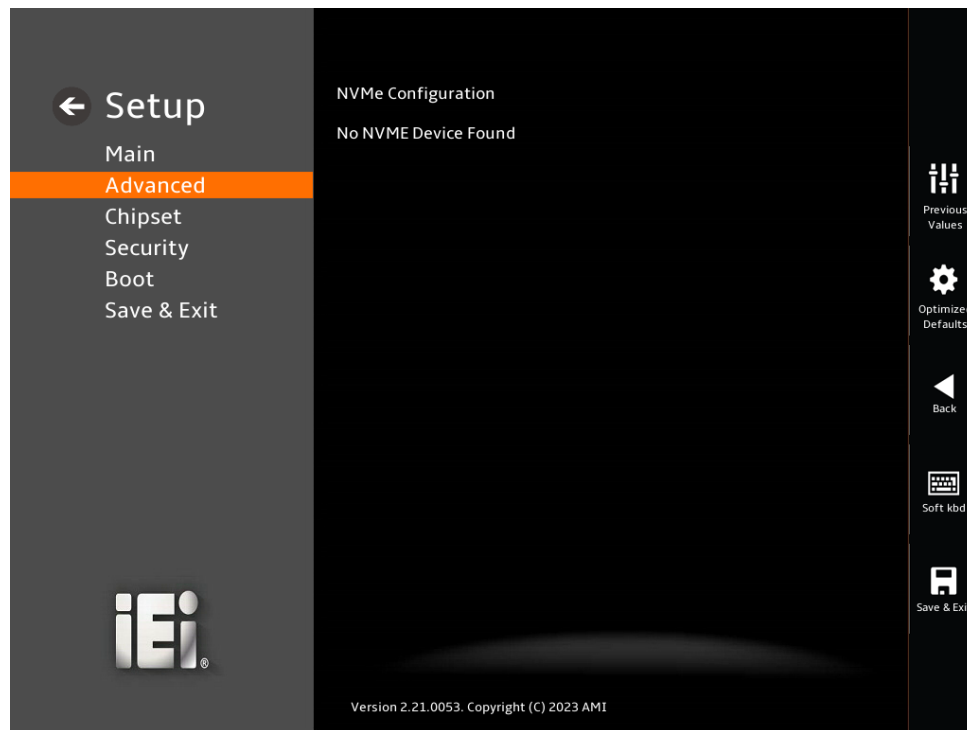
- **1** **DEFAULT** Sets the number of stop bits at 1.

→ 2

Sets the number of stop bits at 2.

5.3.7 NVMe Configuration

Use the **NVMe Configuration (BIOS Menu 16)** menu to display the NVMe controller and device information.



BIOS Menu 16: NVMe Configuration

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5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 17**) to access the PCH IO and System Agent (SA) configuration menus.

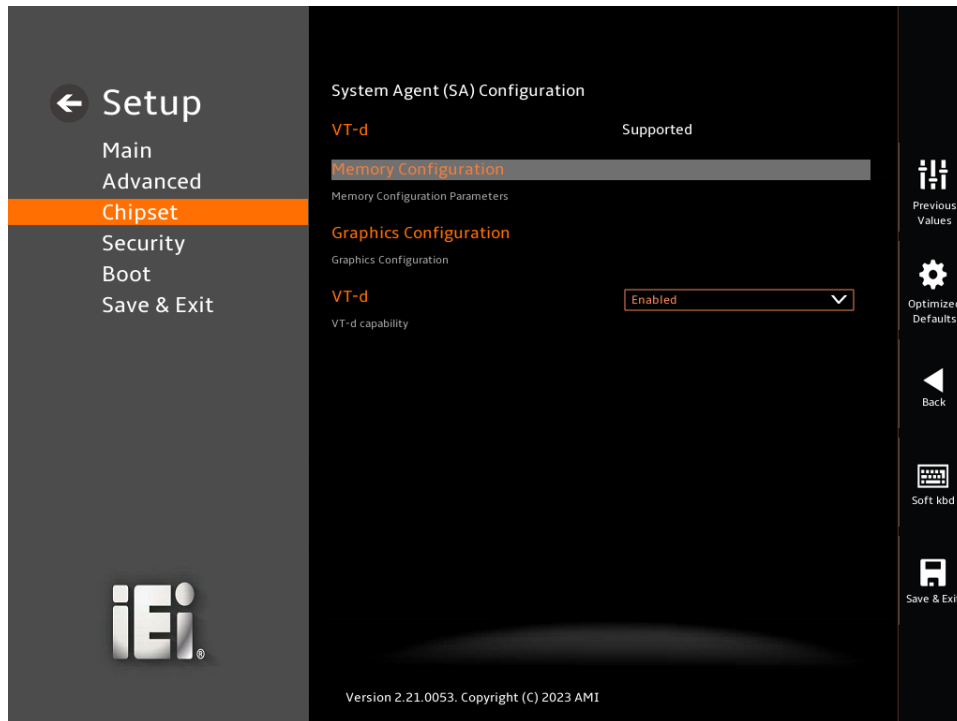
**WARNING!**

Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.

**BIOS Menu 17: Chipset**

5.4.1 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 18**) to configure the System Agent (SA) parameters.



BIOS Menu 18: System Agent (SA) Configuration

➔ **VT-d [Enabled]**

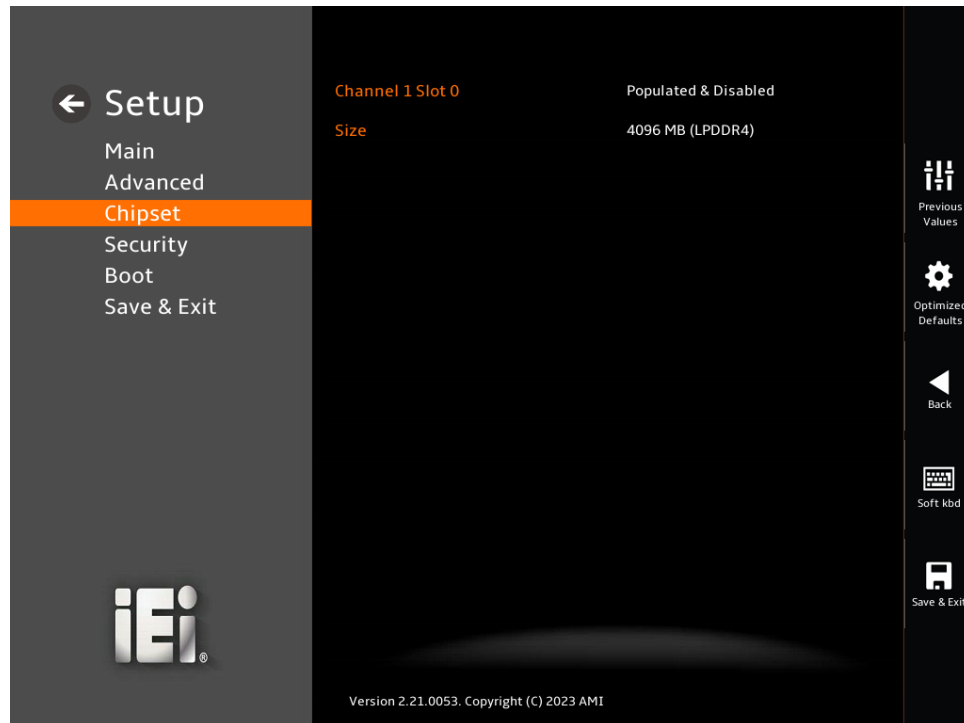
Use the **VT-d** option to enable or disable the VT-d capability.

- ➔ **Disabled** Disable the VT-d capability
- ➔ **Enabled** **DEFAULT** Enable the VT-d capability

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5.4.1.1 Memory Configuration

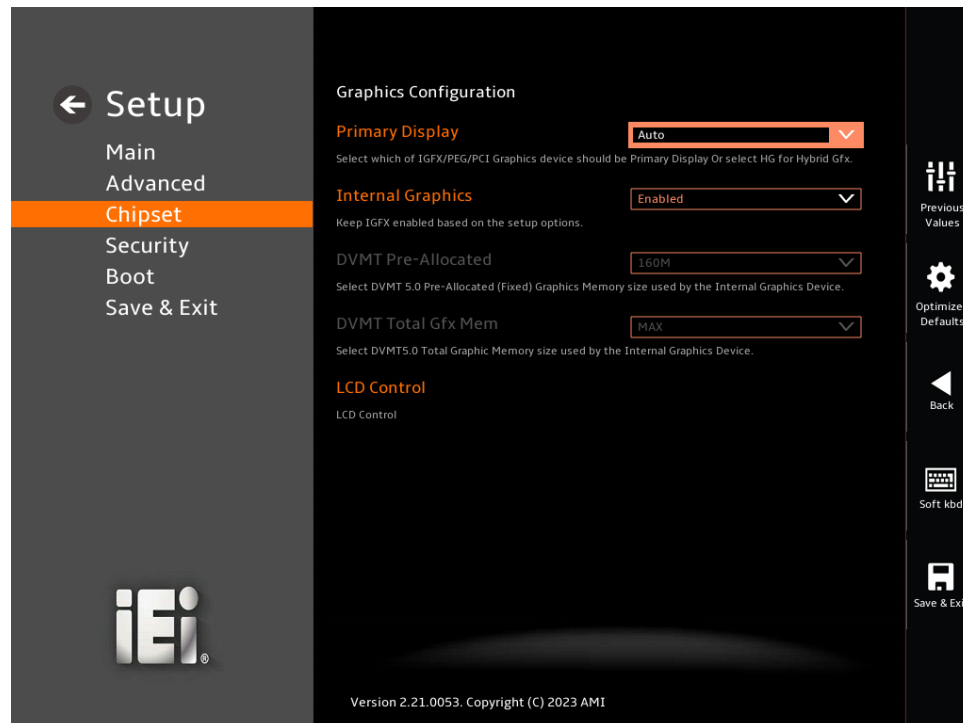
Use the **Memory Configuration** submenu (**BIOS Menu 19**) to view memory information.



BIOS Menu 19: Memory Configuration

5.4.1.2 Graphics Configuration

Use the **Graphics Configuration (BIOS Menu 20)** menu to configure the video device connected to the system.



BIOS Menu 20: Graphics Configuration

→ Primary Display [Auto]

Use the **Primary Display** option to select the primary graphics controller the system uses. The following options are available:

- Auto **Default**
- IGFX
- PEG
- PCI
- SG

→ Internal Graphics [Enabled]

Use the **Internal Graphics** option to configure whether to keep IGFX enabled. If user wants to support dual display by internal graphics and external graphics, this Internal

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Graphics option should be set to Enabled and the above Primary Display option should be set to IGFX.

- **Auto** Auto mode
- **Disabled** Disables IGFX.
- **Enabled** **Default** Enables IGFX.

→ DVMT Pre-Allocated [160M]

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

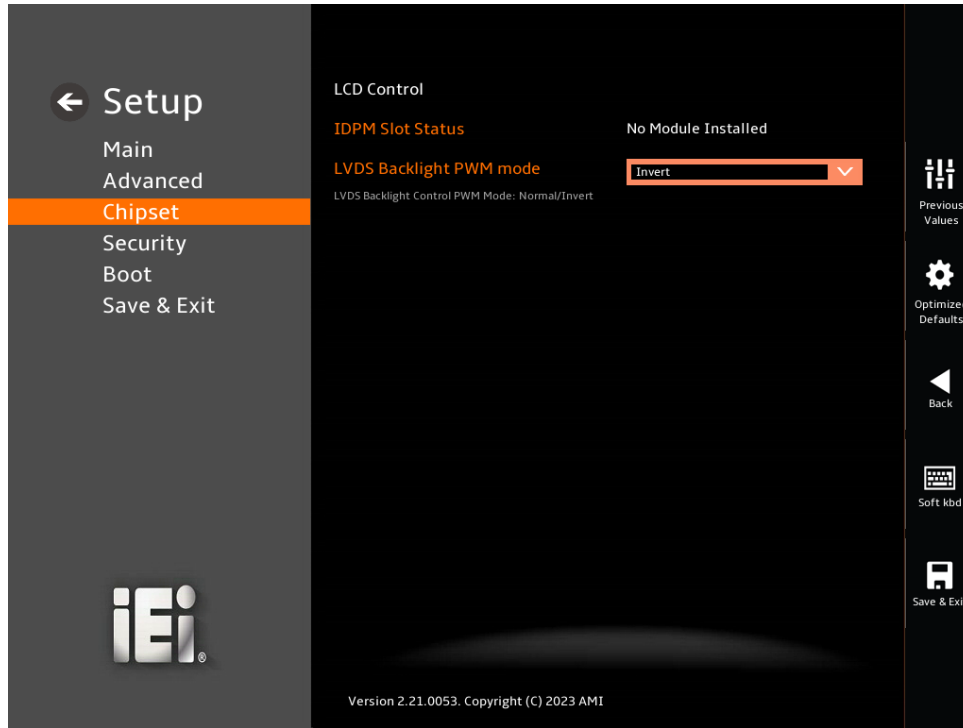
- 80M
- 160M **Default**

→ DVMT Total Gfx Mem [MAX]

Use the **DVMT Total Gfx Mem** option to select DVMT5.0 total graphic memory size used by the internal graphic device. The following options are available:

- 128M
- 256M
- MAX **Default**

➔ **LCD Control**



BIOS Menu 21: LCD Control

➔ **LVDS Backlight PWM mode [Invert]**

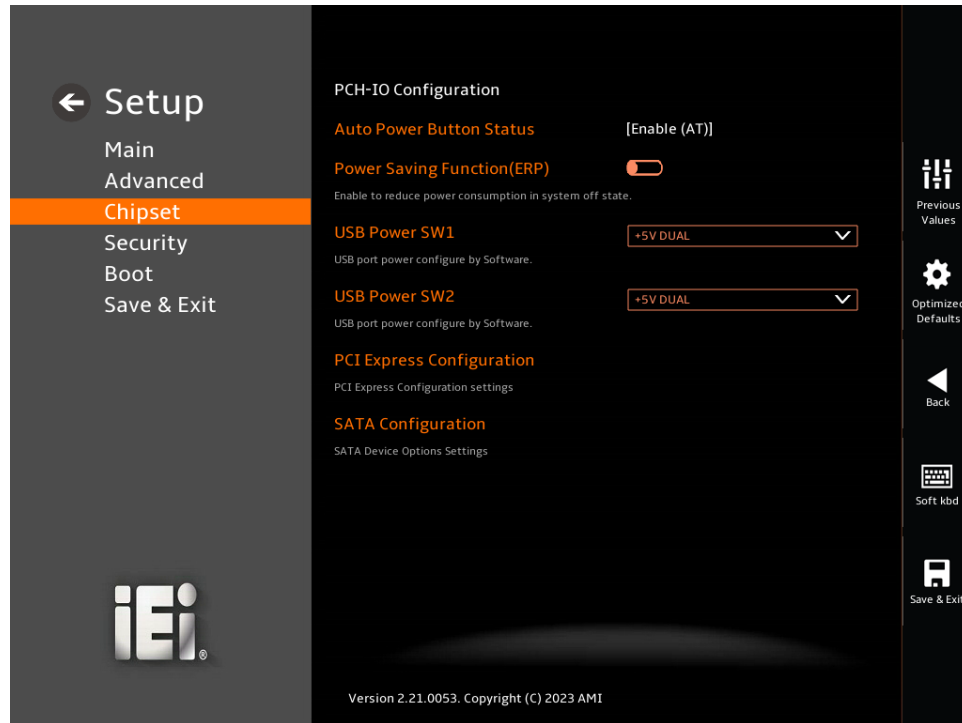
Use the **LVDS Backlight PWM mode** option to specify a PWM mode for LVDS backlight control.

- ➔ **Invert** **Default** Set to invert LVDS Backlight
- ➔ **Normal** Set to normal LVDS Backlight.

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5.4.2 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 22**) to configure the PCH parameters.



BIOS Menu 22: PCH-IO Configuration

➔ **Auto Power Button Function [Disabled (ATX)]**

Use the **Auto Power Button Function** BIOS option to show the power mode state. Use the **J_ATX_AT1** to switch the AT/ATX power mode.

- ➔ **Enabled (AT)** The system power mode is AT.
- ➔ **Disabled (ATX)** **DEFAULT** The system power mode is ATX.

➔ **Power Saving Function (ERP) [Disabled]**

Use the **Power Saving Function (ERP)** BIOS option to enable or disable the power saving function.

- ➔ **Disabled** **DEFAULT** Power saving function is disabled.

➔ **Enabled**

Power saving function is enabled. It will reduce power consumption when the system is off.

➔ **USB Power state [+5VDUAL]**

Use the **USB Power state option** to enable or disable the USB Power.

➔ **+5VDUAL** **DEFAULT** USB Power is on.

➔ **+5** USB Power is off.

5.4.2.1 PCI Express Configuration

Use the **PCI Express Configuration** submenu (**BIOS Menu 23**) to configure the PCI Express slots.



BIOS Menu 23: PCI Express Configuration

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5.4.2.1.1 PCIe Root Port Setting

Use the **PCIEX4_1X4, M2_B1** submenu (**BIOS Menu 24**) to configure the PCIe Root Port Setting.



BIOS Menu 24: PCIe Slot Configuration Submenu

→ PCIe Speed [Auto]

Use the **PCIe Speed** option to specify the PCI Express port speed. Configuration options are listed below.

- | | | | |
|---|-------------|----------------|-------------------------------|
| → | Auto | DEFAULT | Auto mode. |
| → | Gen1 | | Configure PCIe Speed to Gen1. |
| → | Gen2 | | Configure PCIe Speed to Gen2. |
| → | Gen3 | | Configure PCIe Speed to Gen3. |

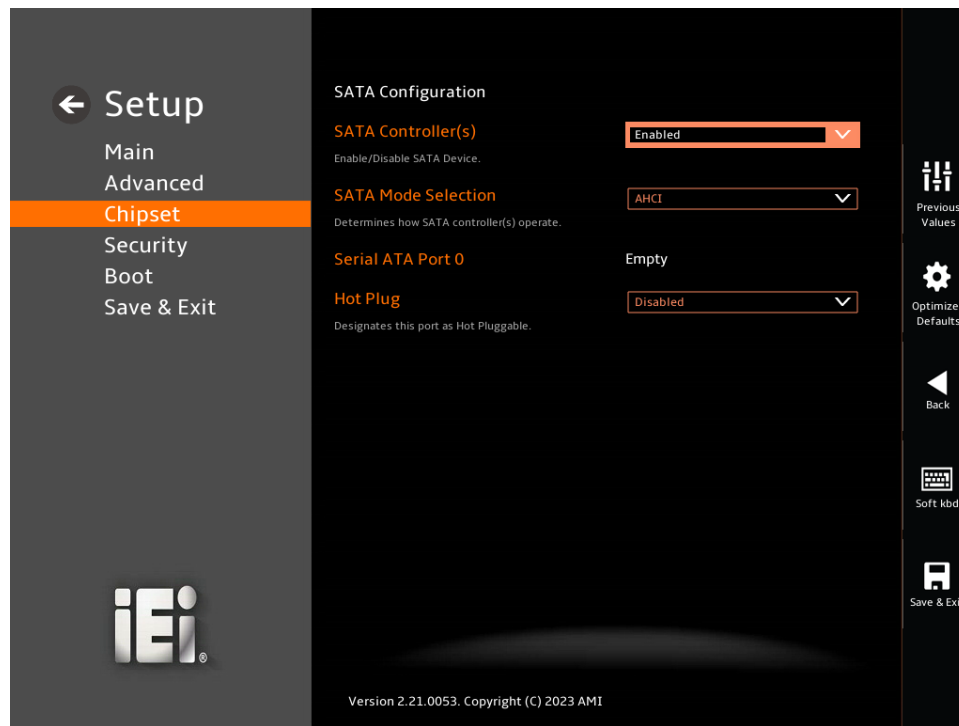
➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to configure whether to detect if a non-compliance PCI Express device is connected to the PCI Express port.

- ➔ **Disabled** **DEFAULT** Do not detect if a non-compliance PCI Express device is connected to the PCI Express port.
- ➔ **Enabled** Detect if a non-compliance PCI Express device is connected to the PCI Express port.

5.4.2.2 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 25**) to change and/or set the configuration of the SATA devices installed in the system.



BIOS Menu 25: SATA Configuration

➔ **SATA Controller(s) [Enabled]**

Use the **SATA Controller(s)** option to designate the correspondent port as hot-pluggable.

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- ➔ **Disabled** Disable the SATA device.
- ➔ **Enabled** **DEFAULT** Enable the SATA device.

➔ **SATA Mode Selection [AHCI]**

Use the **SATA Mode Selection** option to determine how the SATA devices operate.

- ➔ **AHCI** **DEFAULT** Configures SATA devices as AHCI device.
- ➔ **Intel RST Premium
With Intel Optane
System Acceleration** Configures SATA devices to the Intel RST Premium With Intel Optane System Acceleration mode.

➔ **Hot Plug [Disabled]**

Use the **Hot Plug** option to designate the correspondent port as hot-pluggable.

- ➔ **Disabled** **DEFAULT** Disables the hot-pluggable function of the SATA port.
- ➔ **Enabled** Designates the SATA port as hot-pluggable.

5.5 Security

Use the **Security** menu (**BIOS Menu 27**) to set system and user passwords.



BIOS Menu 26: Security (1/2)

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BIOS Menu 27: Security (2/2)

→ Administrator Password

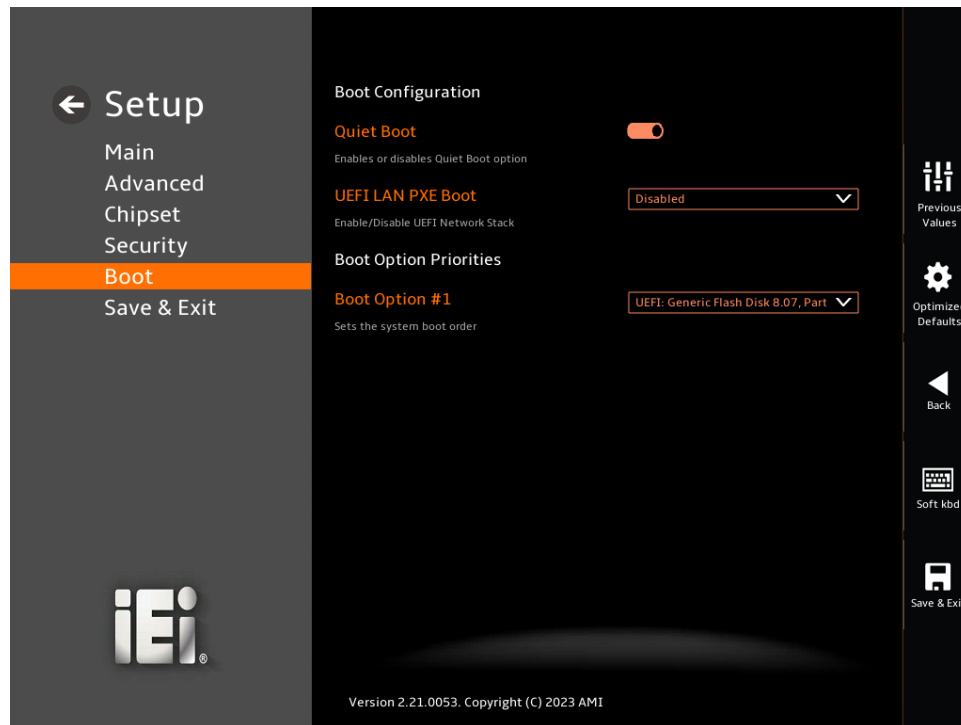
Use the **Administrator Password** to set or change an administrator password.

→ User Password

Use the **User Password** to set or change a user password.

5.6 Boot

Use the **Boot** menu (**BIOS Menu 28**) to configure system boot options.



BIOS Menu 28: Boot

5.6.1 Boot Configuration

→ Quiet Boot [Enabled]

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

- **Disabled** Normal POST messages displayed
- **Enabled** **DEFAULT** OEM Logo displayed instead of POST messages

→ Launch PXE OpROM [Disabled]

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

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- ➔ **Disabled** **DEFAULT** Ignore all PXE Option ROMs
- ➔ **Enabled** Load PXE Option ROMs.

➔ **Option ROM Messages [Force BIOS]**

Use the **Option ROM Messages** option to set the Option ROM display mode.

- ➔ **Force BIOS** **DEFAULT** Sets display mode to force BIOS.
- ➔ **Keep Current** Sets display mode to current.

5.6.2 Boot Option Priorities

Use the Boot Option # N to choose the system boots from the peripherals you selected. The following Boot Options are listed as an example.

➔ **Boot Option #1**

Sets the system boot order **ADATA SP580** as the first priority.

- ➔ **Windows Boot Manager (P1: ADATA SSD SP580 240GB)**
- ➔ **Disabled**

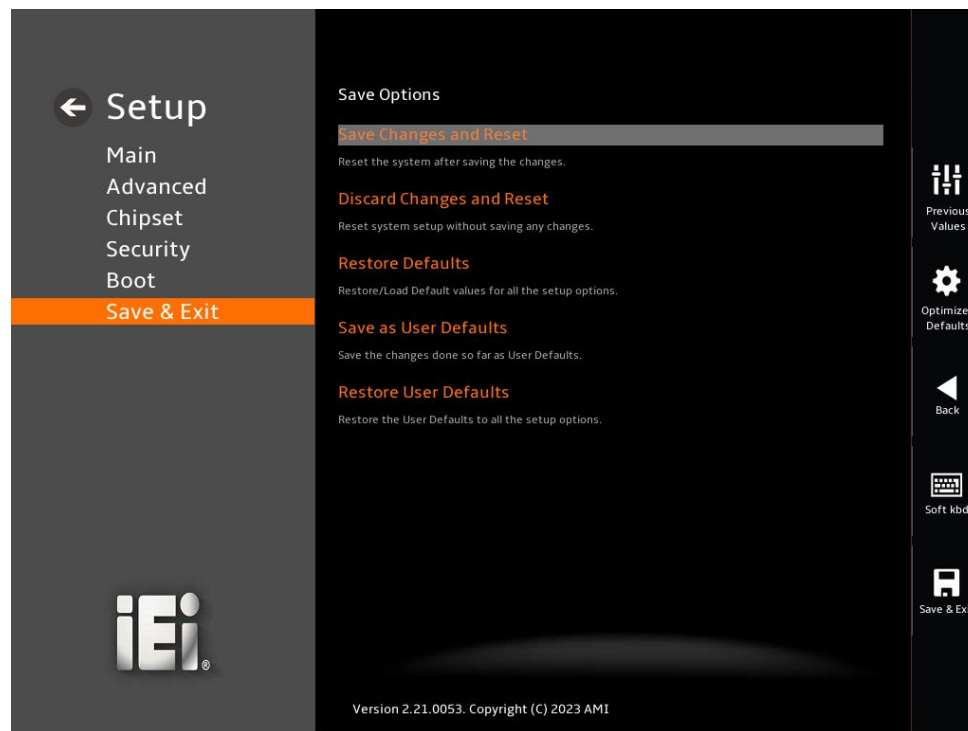
➔ **Boot Option #2**

Sets the system boot order **USB Partition 1** as the second priority.

- ➔ **UEFI: USB, Partition 1**
- ➔ **Disabled**

5.7 Save & Exit

Use the **Save & Exit** menu (**BIOS Menu 29**) to load default BIOS values, optimal failsafe values and to save configuration changes.



BIOS Menu 29: Save & Exit

→ Save Changes and Reset

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

→ Discard Changes and Reset

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

→ Restore Defaults

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

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→ Save as User Defaults

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

→ Restore User Defaults

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Appendix

A

Regulatory Compliance

HYPER-EHL

DECLARATION OF CONFORMITY



This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING



This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications.

Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

Product Disposal

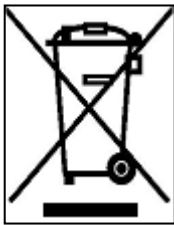
HYPER-EHL

**CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union–If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union–The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

BIOS Options

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Below is a list of BIOS configuration options in the BIOS chapter.

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➔ System Time [xx:xx:xx].....	67
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➔ Active Processor Cores [All]	71
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➔ C states [Disabled].....	71
➔ Tcc Activation Offset [0].....	72
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➔ Power Limit 1 Time Window [0].....	72
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➔ Console Redirection [Disabled].....	79
➔ Terminal Type [ANSI].....	80
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➔ Data Bits [8]	81
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➔ DVMT Pre-Allocated [160M]	87
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→ Power Saving Function (ERP) [Disabled]	89
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Appendix

D

Watchdog Timer



NOTE:

The following discussion applies to DOS environment. Contact IEI support or visit the IEI website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer’s period.
BL:	Time-out value (Its unit-second is dependent on the item “Watchdog Timer unit select” in CMOS setup).

Table D-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

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**NOTE:**

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

EXAMPLE PROGRAM:

; INITIAL TIMER PERIOD COUNTER

;

W_LOOP:

;

```

MOV      AX, 6F02H      ;setting the time-out value
MOV      BL, 30         ;time-out value is 48 seconds
INT      15H

```

;

; ADD THE APPLICATION PROGRAM HERE

;

```

CMP      EXIT_AP, 1     ;is the application over?
JNE      W_LOOP        ;No, restart the application

```

```

MOV      AX, 6F02H      ;disable Watchdog Timer
MOV      BL, 0         ;
INT      15H

```

;

; EXIT ;

Appendix

E

Error Beep Code

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E.1 PEI Beep Codes

Number of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXE IPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

E.2 DXE Beep Codes

Number of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met



NOTE:

If you have any question, please contact IEI for further assistance.

Appendix

F

Hazardous Materials Disclosure

HYPER-EHL

F.1 RoHS II Directive (2015/863/EU)

The details provided in this appendix are to ensure that the product is compliant with the RoHS II Directive (2015/863/EU). The table below acknowledges the presences of small quantities of certain substances in the product, and is applicable to RoHS II Directive (2015/863/EU).

Please refer to the following table.

Part Name	Toxic or Hazardous Substances and Elements									
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)	Bis(2-ethylhexyl) phthalate (DEHP)	Butyl benzyl phthalate (BBP)	Dibutyl phthalate (DBP)	Diisobutyl phthalate (DIBP)
Housing	O	O	O	O	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O	O	O	O	O
Battery	O	O	O	O	O	O	O	O	O	O
<p>O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in Directive (EU) 2015/863.</p> <p>X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in Directive (EU) 2015/863.</p>										

F.2 China RoHS

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有“环境友好使用期限”的标签，此期限是估算这些物质“不会有泄漏或突变”的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	○	○	○	○	○	○
印刷电路板	○	○	○	○	○	○
金属螺帽	○	○	○	○	○	○
电缆组装	○	○	○	○	○	○
风扇组装	○	○	○	○	○	○
电力供应组装	○	○	○	○	○	○
电池	○	○	○	○	○	○
<p>O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求以下。</p> <p>X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求。</p>						