IEI Integration Corp.

MODEL:

PCIE-Q370

Full-Size PICMG 1.3 CPU Card Supports LGA1151 8th Gen. Intel® Core™ i7/i5/i3, Pentium® or Celeron® CPU, Intel® Q370 Chipset, DDR4, DisplayPort, Dual GbE, USB 3.1 Gen1, SATA 6Gb/s, M.2, RS-232, HD Audio and RoHS

User Manual

Rev. 1.10 – March 12, 2019

RoHS Lead Free

Revision

Date	Version	Changes
March 12, 2019	1.10	Modified for R11 version: - Added DisplayPort connector - Added a new SKU: PCIE-Q370-HDMI
September 21, 2018	1.00	Initial release

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Manual Conventions

WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

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Introduction

1.1 Introduction

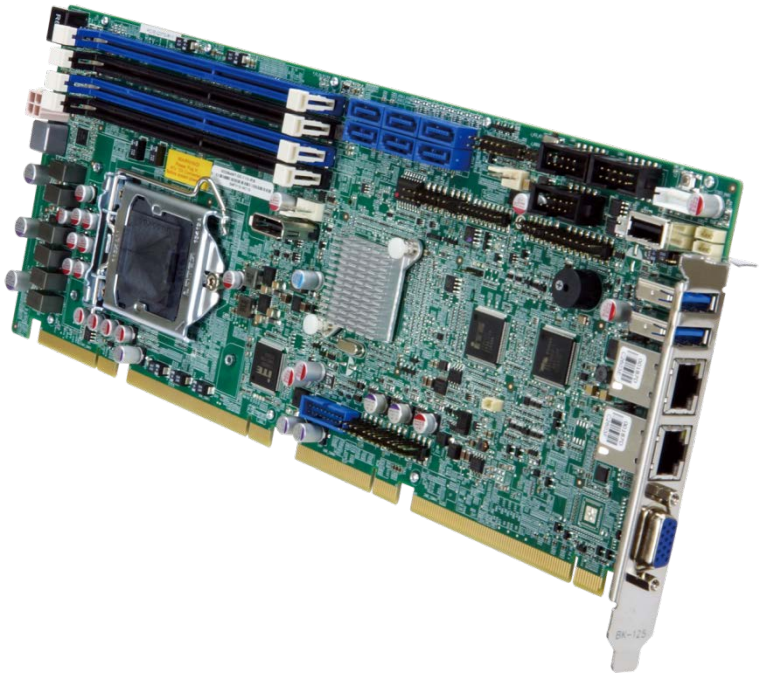


Figure 1-1: PCIE-Q370

The PCIE-Q370 is a full-size PICMG 1.3 CPU card. It accepts a Socket LGA1151 8th generation Intel® Core™ i7/i5/i3, Pentium® or Celeron® processor and supports four 288-pin 2666MHz dual-channel DDR4 DIMM modules up to 64 GB.

The PCIE-Q370 provides two GbE interfaces through the Intel® I219LM (with Intel® AMT 11.0 support) and the Intel® I211AT PCIe controllers. The integrated Intel® Q370 chipset supports six SATA 6Gb/s drives with RAID 0/1/5/10 function.

Two USB 3.1 Gen 1 on the rear panel, two USB 3.1 Gen 1 by internal box header, six USB 2.0 by pin headers, one USB 2.0 by internal Type A connector, three RS-232, one RS-422/485 and one M.2 M-key slot provide flexible expansion options. High Definition Audio (HDA) support ensures HDA devices can be easily implemented on the PCIE-Q370.

1.2 Model Variations

The model variations of the PCIE-Q370 series are listed below.

Model No.	Display Interfaces
PCIE-Q370	One VGA (external) One DisplayPort (onboard)
PCIE-Q370-HDMI*	One HDMI (external) One DisplayPort (onboard)
*By order production, MOQ: 100	

Table 1-1: PCIE-Q370 Model Variations

1.3 Features

The PCIE-Q370 motherboard features are listed below:

- Full-size PICMG 1.3 CPU card
- 8th generation LGA1151 Intel® Core™ i7/i5/i3, Pentium® or Celeron® processor supported
- Intel® Q370 chipset
- Four 288-pin 2666 MHz dual-channel DDR4 DIMMs support up to 64 GB
- Two Intel® PCIe GbE connectors (LAN1 with Intel® AMT 11.0 support)
- Supports PCI Express Generation 3.0
- Supports dual display via DisplayPort and VGA/HDMI
- One M.2 2280 M-key slot for storage
- Six SATA 6Gb/s connectors support RAID 0, 1, 5, 10 function
- Two USB 3.1 Gen 1 (5 Gb/s) ports on the rear I/O
- Two USB 3.1 Gen 1 (5 Gb/s) ports via internal box header
- Six USB 2.0 ports via internal pin headers
- One USB 2.0 via internal Type A connector
- Three RS-232 serial ports
- One RS-422/485 serial port
- TPM V1.2 hardware security function supported by TPM module
- High Definition Audio
- RoHS compliant

1.4 Connectors

The connectors on both of the PCIE-Q370 SKUs are shown in the figures below.

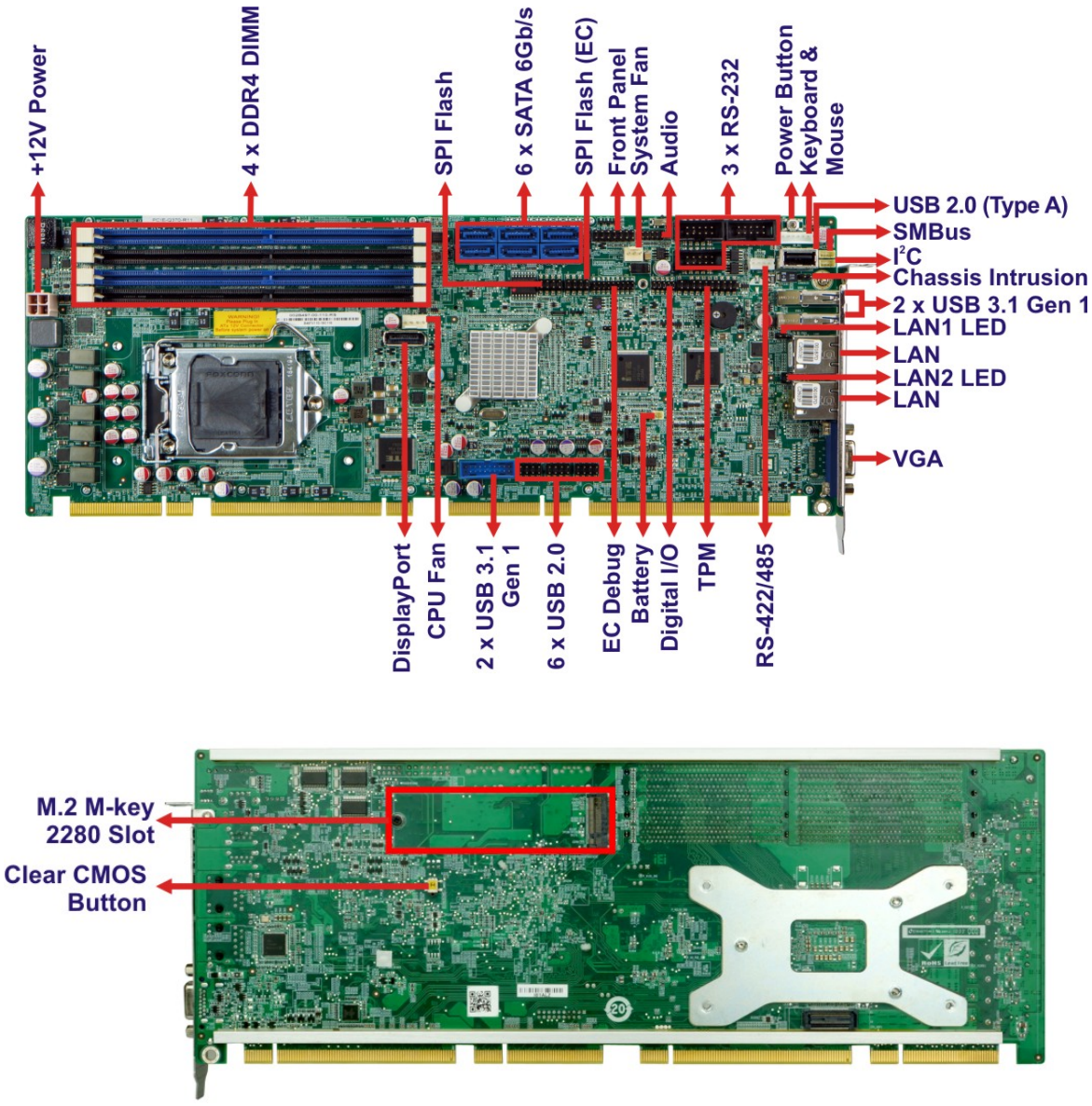


Figure 1-2: PCIE-Q370 Connectors

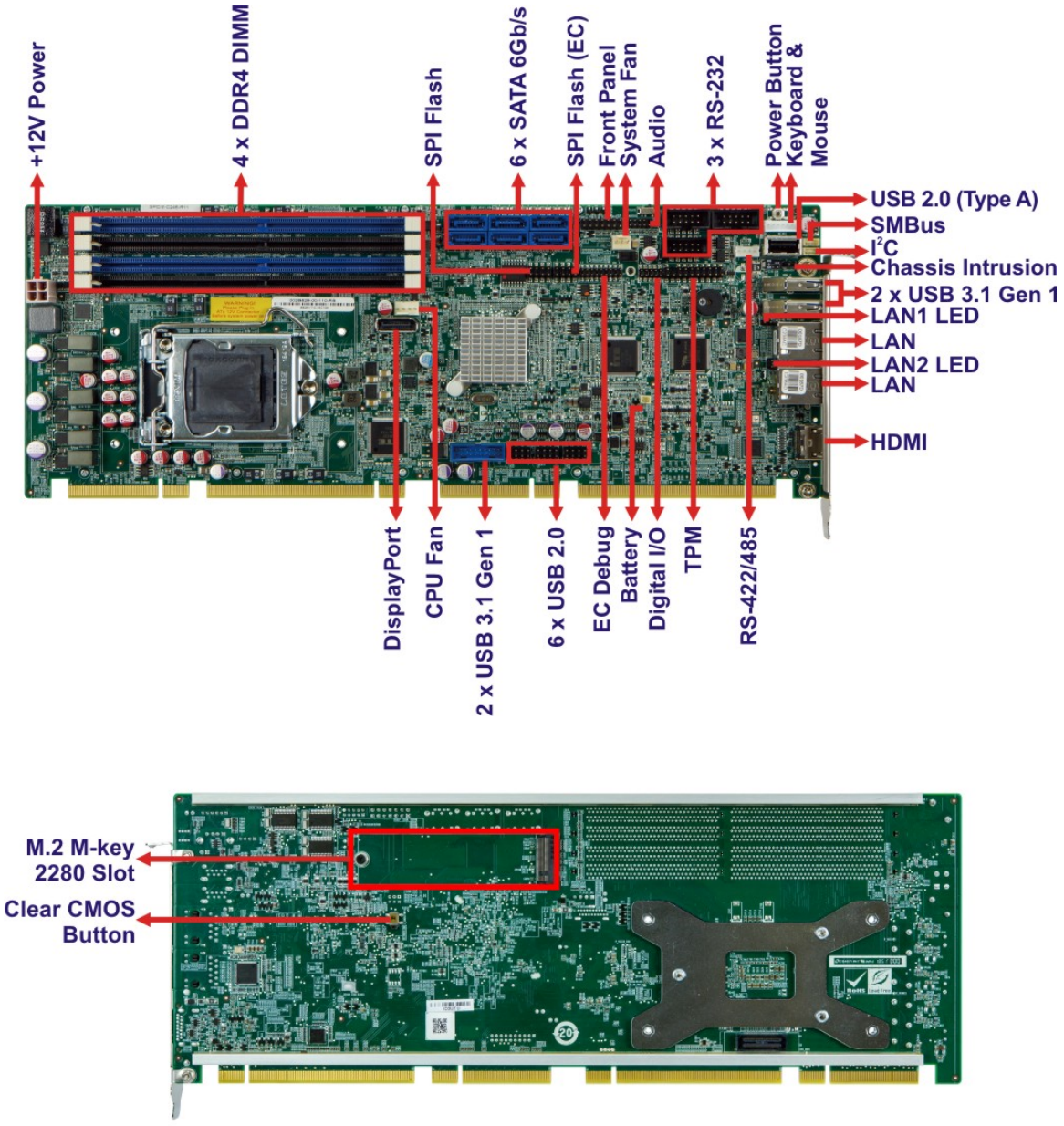


Figure 1-3: PCIE-Q370-HDMI Connectors

1.5 Dimensions

The main dimensions of the PCIE-Q370 are shown in the diagrams below.

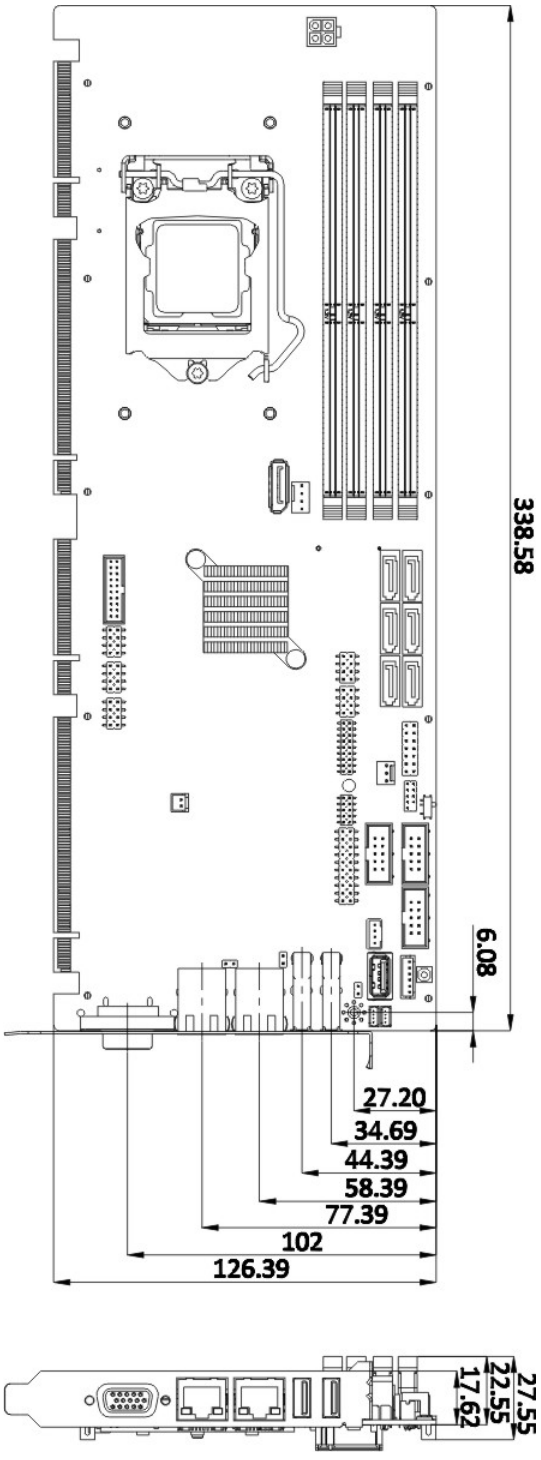


Figure 1-4: PCIE-Q370 Dimensions (mm)

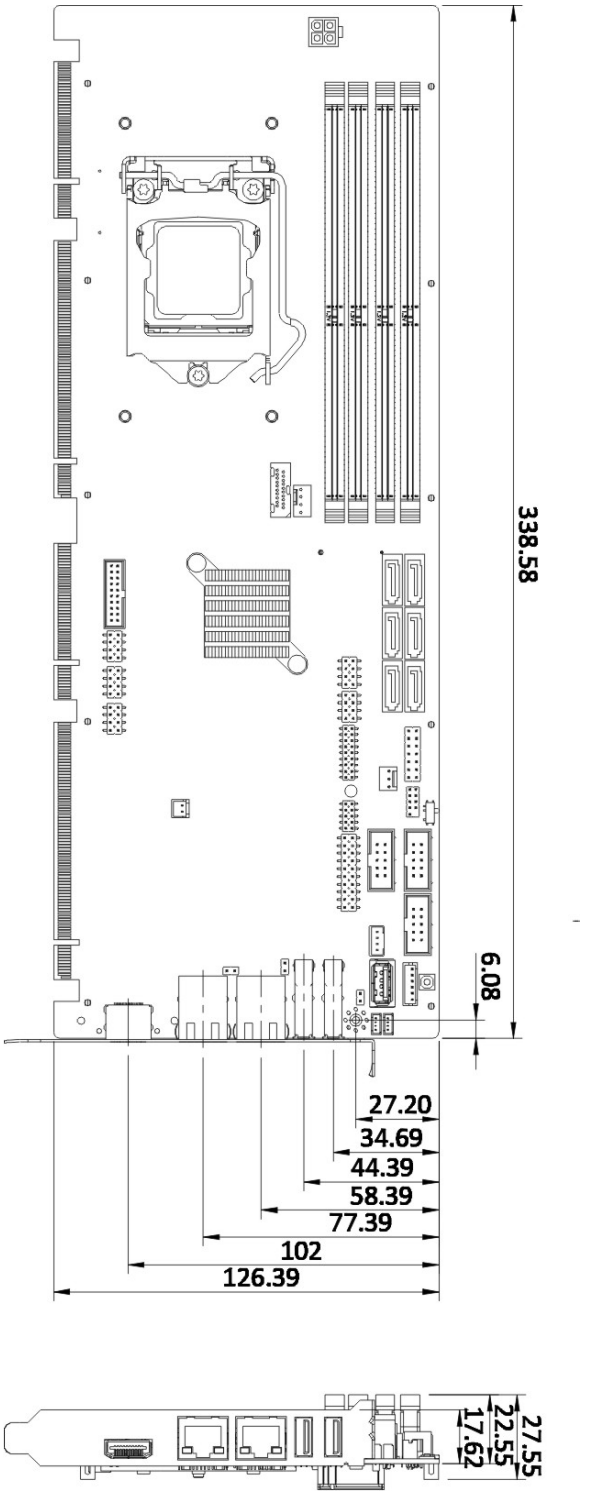


Figure 1-5: PCIE-Q370-HDMI Dimensions (mm)

1.6 Data Flow

Figure 1-6 shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

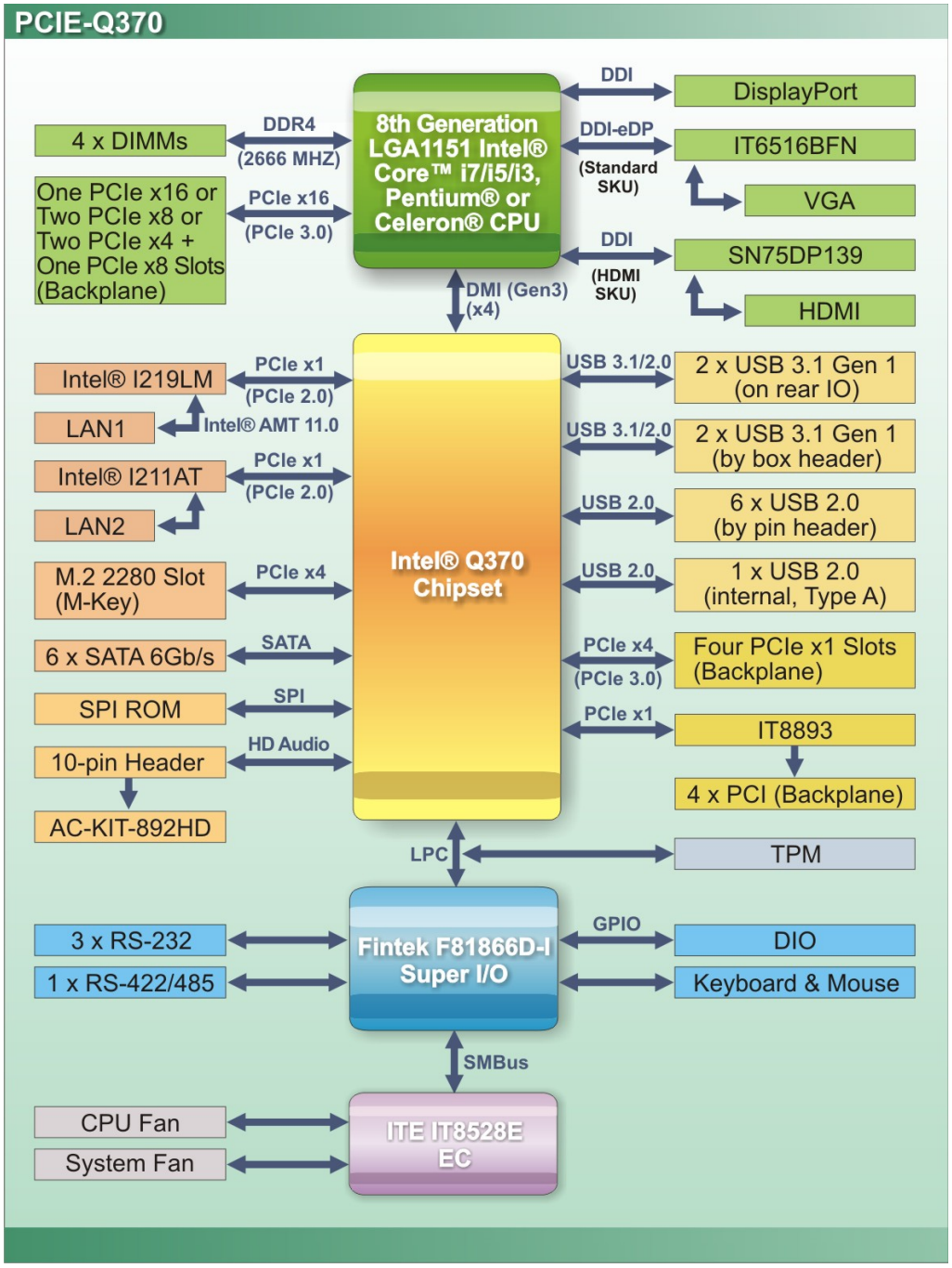


Figure 1-6: Data Flow Diagram

1.7 Technical Specifications

The PCIE-Q370 technical specifications are listed below.

Specification/Model	PCIE-Q370
Form Factor	Full-size PICMG 1.3 CPU card
CPU Supported	8th generation LGA1151 Intel® Core™ i7/i5/i3, Pentium® or Celeron® CPU
PCH	Intel® Q370
Memory	Four 288-pin 2666 MHz dual-channel unbuffered DDR4 SDRAM DIMMs supported (system max. 64 GB)
Graphics Engine	Intel® HD Graphics Gen9 engine with 16 low-power execution units, supporting DX 2015, OpenGL 5.x and OpenCL 2.x, ES 2.0
Display Output	One DisplayPort (up to 4096 x 2304 @ 60Hz) One VGA (via IT6516BFN, up to 1920x1200 @ 60Hz) **or** one HDMI (up to 4096 x 2304 @ 30Hz)
Ethernet Controllers	**LAN1**: Intel® I219LM PHY with Intel® AMT 11.0 support **LAN2**: Intel® I211AT PCIe GbE controller (colay I210AT)
Audio	Supports 7.1-channel HD audio by IEI AC-KIT-892HD kit
BIOS	UEFI BIOS
Expansions	**One M.2 2280 slot** (M key, PCIe x4 only) **4 x PCI link via golden finger** **4 x PCIe x1 link via golden finger** **16-lane PCIe link from CPU via golden finger:** Supports one PCIe x16, or two PCIe x8, or two PCIe x4 + one PCIe x8 slots on the backplane (configured via BIOS)
Super I/O Controller	Fintek F81866D-I
Embedded Controller	ITE IT8528E
Watchdog Timer	Software programmable supports 1~255 sec. system reset
I/O Interface Connectors	
Audio Connector	One audio connector (10-pin header)
Chassis Intrusion	One 2-pin header
Digital I/O	8-bit digital I/O (10-pin header)

Ethernet	Two RJ-45 ports
Fan	One 4-pin CPU smart fan connector One 3-pin system smart fan connector
Front Panel	One 14-pin header (power LED, HDD LED, speaker, power button, reset button)
I^2C	One 4-pin wafer connector
Keyboard and Mouse	One internal keyboard and mouse connector (6-pin wafer)
LAN LED	Two 2-pin headers for LAN1 LED and LAN2 LED
Serial ATA	Six SATA 6Gb/s connectors (support RAID 0, 1, 5, 10)
Serial Ports	Three RS-232 via internal 10-pin box headers One RS-422/485 via internal 4-pin wafer
SMBus	One 4-pin wafer connector
TPM	One via 20-pin header
USB 2.0	Six USB 2.0 ports by three internal pin headers One USB 2.0 port by internal Type A connector
USB 3.1 Gen 1 (5 Gb/s)	Two USB 3.1 Gen 1 ports on rear panel Two USB 3.1 Gen 1 ports via internal box header
Environmental and Power Specifications	
Power Supply	AT/ATX power support ErP/EuP compliant
Power Consumption	5V@3.12A, 12V@6.85A, 3.3V@1.13A, 5VSB@0.15A (4.0 GHz Intel® Core™ i7-8700K CPU with four 16 GB 2666 MHz DDR4 memory)
Operating Temperature	-20ºC ~ 60ºC
Storage Temperature	-30ºC ~ 70ºC
Operating Humidity	5% ~ 95% (non-condensing)
Safety/EMC	CE, FCC
Physical Specifications	
Dimensions	338 mm x 126 mm
Weight (GW/NW)	1000 g/500 g

Table 1-2: PCIE-Q370 Specifications

Chapter

2

Packing List

2.1 Anti-static Precautions

WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- ***Wear an anti-static wristband***: Wearing an anti-static wristband can prevent electrostatic discharge.
- ***Self-grounding***: Touch a grounded conductor every few minutes to discharge any excess static buildup.
- ***Use an anti-static pad***: When configuring any circuit board, place it on an anti-static mat.
- ***Only handle the edges of the PCB***: Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the PCIE-Q370 is unpacked, please do the following:

- Follow the anti-static guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

2.3 Packing List

NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the PCIE-Q370 was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

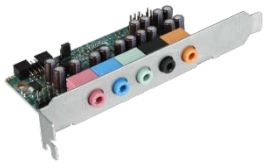
The PCIE-Q370 is shipped with the following components:

Quantity	Item and Part Number	Image
1	PCIE-Q370 CPU card	
1	SATA cable	
1	Mini jumper pack	
1	Quick installation guide	

Table 2-1: Packing List

2.4 Optional Items

The following are optional components which may be separately purchased:

Item and Part Number	Image
PS/2 KB/MS Y-cable with bracket (**P/N**: 19800-000075-RS)	
SATA power cable (**P/N**: 32102-000100-200-RS)	
7.1-channel HD audio kit with Realtek ALC892 audio codec supporting dual audio stream (**P/N**: AC-KIT-892HD-R10)	
LGA1150 cooler kit (high-performance compatible, 95W) (**P/N**: CF-1150SA-R10)	
LGA1150 cooler kit (high-performance compatible, 65W) (**P/N**: CF-1150SB-R11)	
LGA1150 cooler kit (1U chassis compatible, 65W) (**P/N**: CF-1150SC-R20)	
LGA1150 cooler kit (high-performance compatible, 95W) (**P/N**: CF-1150SE-R11)	

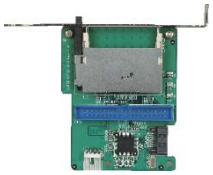
Item and Part Number	Image
LGA1150 cooler kit (1U chassis compatible, 54W) (**P/N**: CF-1150SF-R10)	
SATA to IDE/CompactFlash® converter board (**P/N**: SAIDE-KIT01-R10)	

Table 2-2: Optional Items

Chapter

3

Connectors

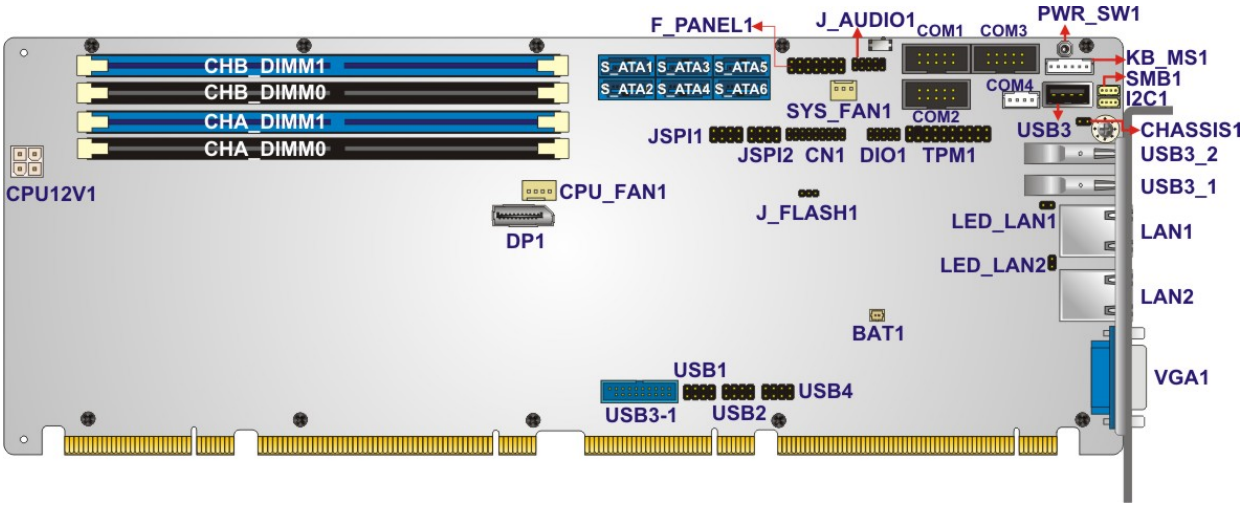
3.1 Peripheral Interface Connectors

This chapter details all the peripheral interface connectors.

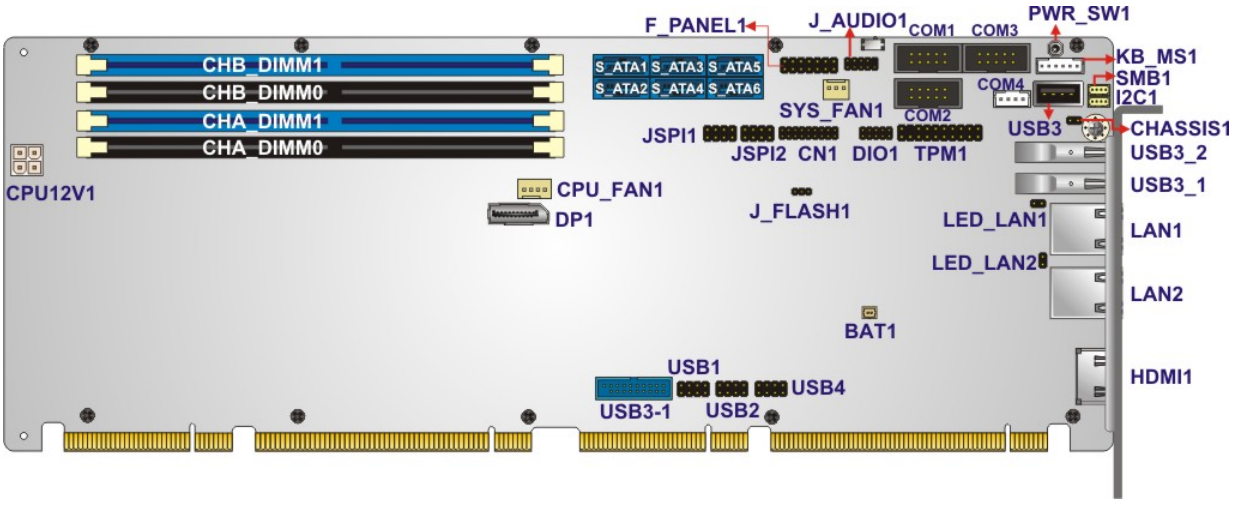
3.1.1 PCIE-Q370 Layout

The figure below shows all the peripheral interface connectors.

PCIE-Q370



PCIE-Q370-HDMI



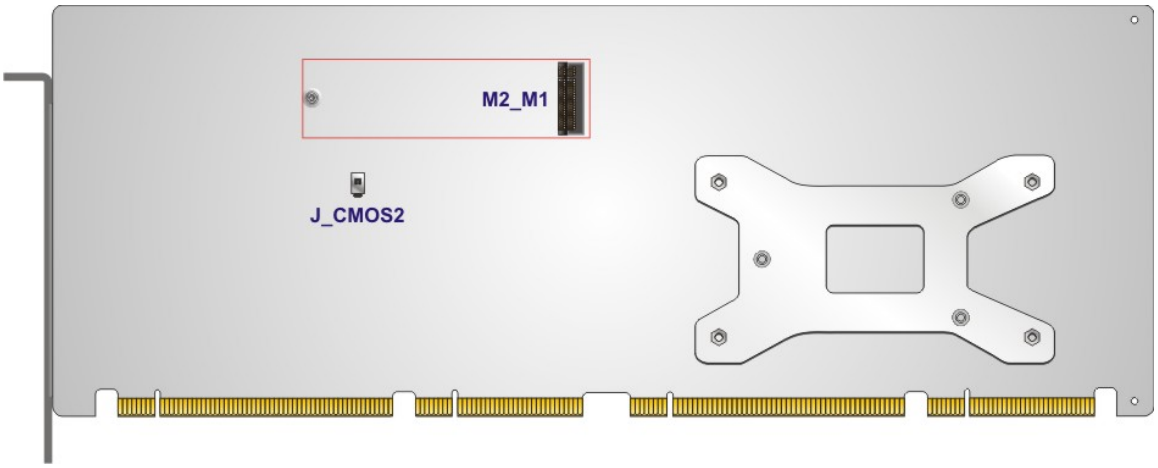


Figure 3-1: Peripheral Interface Connectors

3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
+12V ATX power supply connector	4-pin Molex power connector	CPU12V1
Audio kit connector	10-pin header	J_AUDIO1
Battery connector	2-pin wafer	BAT1
Chassis intrusion connector	2-pin header	CHASSIS1
DDR4 DIMM sockets	288-pin socket	CHA_DIMM0, CHA_DIMM1, CHB_DIMM0, CHB_DIMM1
Digital I/O connector	10-pin header	DIO1
DisplayPort connector	20-pin DP port	DP1
EC debug connector	18-pin header	CN1
Fan connector (CPU)	4-pin wafer	CPU_FAN1
Fan connector (system)	3-pin wafer	SYS_FAN1
Front panel connector	14-pin header	F_PANEL1
I^2C connector	4-pin wafer	I2C1
Keyboard and mouse connector	6-pin wafer	KB_MS1
LAN LED connectors	2-pin header	LED_LAN1, LED_LAN2
M.2 M-key slot	M.2 M-key 2280	M2_M1
Power button	Push button	PWR_SW1
RS-232 serial ports	10-pin box header	COM1, COM2, COM3,
RS-422/485 serial port	4-pin wafer	COM4

Connector	Type	Label
SATA 6Gb/s drive connector	7-pin SATA connector	S_ATA1, S_ATA2, S_ATA3, S_ATA4, S_ATA5, S_ATA6,
SMBus connector	4-pin wafer	SMB1
SPI flash connector	8-pin header	JSPI1
SPI flash connector, EC	8-pin header	JSPI2
TPM connector	20-pin header	TPM1
USB 2.0 connectors	8-pin header	USB1, USB2, USB4
USB 2.0 connector (Type A)	Type A	USB3
USB 3.1 Gen 1 connector	19-pin box header	USB3-1

Table 3-1: Peripheral Interface Connectors

3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
Ethernet ports	RJ-45	LAN1, LAN2
USB 3.1 Gen 1 ports	USB 3.1 Gen 1	USB3_1, USB3_2
VGA connector (standard SKU only)	15-pin female	VGA1
HDMI connector (HDMI SKU only)	HDMI port	HDMI1

Table 3-2: External Peripheral Connectors

3.2 Internal Peripheral Connectors

The section describes all of the connectors on the PCIE-Q370.

3.2.1 +12V ATX Power Connector

CN Label: **CPU12V1**

CN Type: 4-pin Molex power connector, p=4.2 mm

CN Location: See **Figure 3-2**

CN Pinouts: See **Table 3-3**

This connector provides power to the CPU.

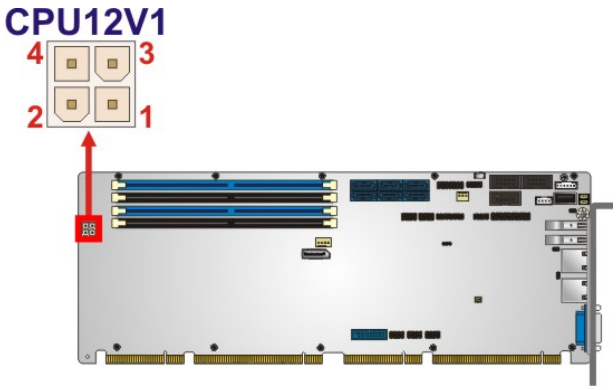


Figure 3-2: +12V ATX Power Connector Pinout Location

Pin	Description	Pin	Description
1	GND	2	GND
3	+12V	4	+12V

Table 3-3: +12V ATX Power Connector Pinouts

3.2.2 Audio Kit Connector

CN Label: **J_AUDIO1**

CN Type: 10-pin header, p=2.00 mm

CN Location: See **Figure 3-3**

CN Pinouts: See **Table 3-4**

This connector allows connection to an external audio kit.

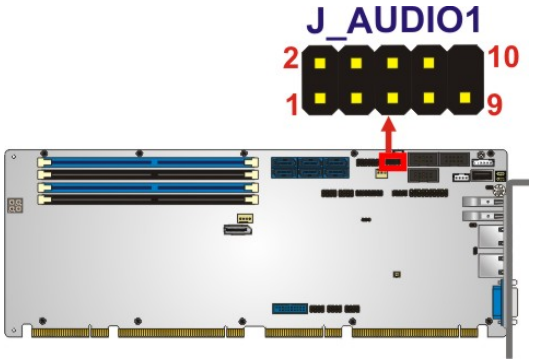


Figure 3-3: Audio Connector Location

Pin	Description	Pin	Description
1	HDA_SYNC	2	HDA_BIT_CLK
3	HDA_SDOUT	4	HDA_SPKR
5	HDA_SDIN	6	HDA_RST#
7	HDA_VCC	8	HDA_GND
9	HDA_+12V	10	HDA_GND

Table 3-4: Audio Connector Pinouts

3.2.3 Battery Connector

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

NOTE:

It is recommended to attach the RTC battery onto the system chassis in which the PCIE-Q370 is installed.

CN Label:	**BAT1**
CN Type:	2-pin wafer, p=1.25 mm
CN Location:	See **Figure 3-4**
CN Pinouts:	See **Table 3-5**

This is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.

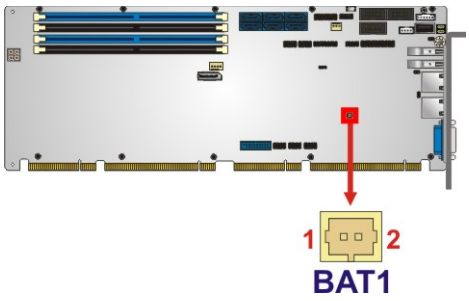


Figure 3-4: Battery Connector Location

Pin	Description
1	VBATT
2	GND

Table 3-5: Battery Connector Pinouts

3.2.4 Chassis Intrusion Connector

CN Label: **CHASSIS1**

CN Type: 2-pin header, p=2.54 mm

CN Location: See **Figure 3-5**

CN Pinouts: See **Table 3-6**

The chassis intrusion connector is for a chassis intrusion detection sensor or switch that detects if a chassis component is removed or replaced.

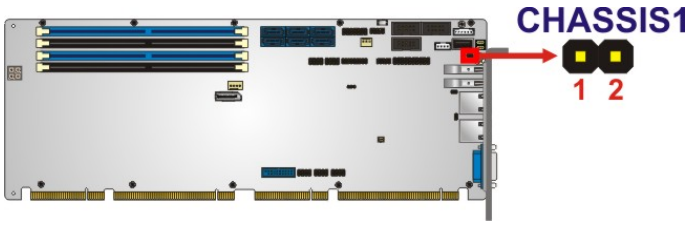


Figure 3-5: Chassis Intrusion Connector Location

Pin	Description
1	+3.3VSB
2	CHASSIS OPEN

Table 3-6: Chassis Intrusion Connector Pinouts

3.2.5 DDR4 DIMM Sockets

CN Label: **CHA_DIMM0, CHA_DIMM1, CHB_DIMM0, CHB_DIMM1**

CN Type: 288-pin DDR4 DIMM socket

CN Location: See **Figure 3-6**

The DIMM sockets are for DDR4 DIMM memory modules.

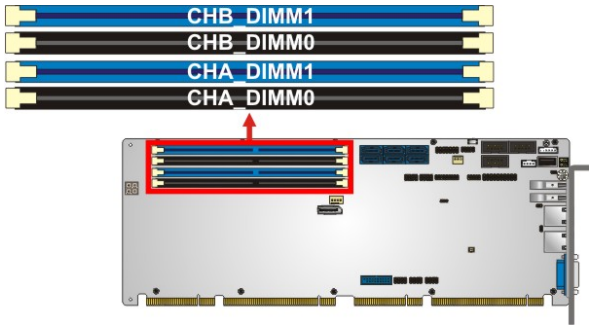


Figure 3-6: DDR4 DIMM Socket Locations

3.2.6 Digital I/O Connector

CN Label: **DIO1**

CN Type: 10-pin header, p=2.00 mm

CN Location: See **Figure 3-7**

CN Pinouts: See **Table 3-7**

The digital I/O connector provides programmable input and output for external devices.

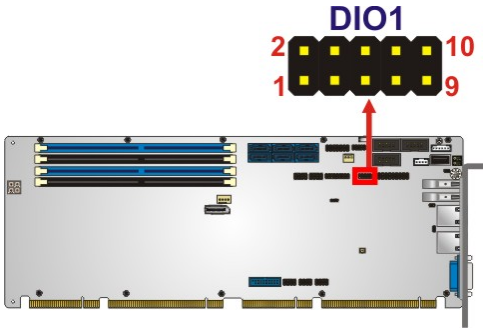


Figure 3-7: Digital I/O Connector Location

Pin	Description	Pin	Description
1	GND	2	VCC
3	Output 3	4	Output 2
5	Output 1	6	Output 0
7	Input 3	8	Input 2
9	Input 1	10	Input 0

Table 3-7: Digital I/O Connector Pinouts

3.2.7 DisplayPort Connector

CN Label: **DP1**

CN Type: 20-pin DisplayPort

CN Location: See **Figure 3-8**

CN Pinouts: See **Table 3-8**

The DisplayPort connector connects to a display device with DisplayPort interface.

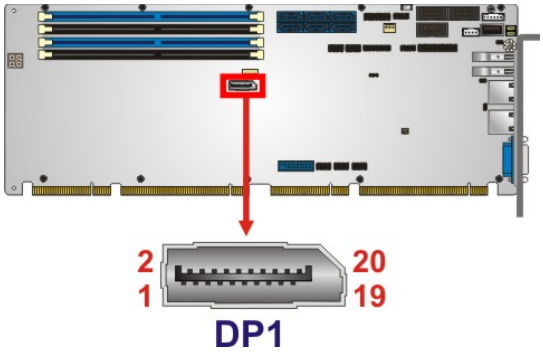


Figure 3-8: DisplayPort Connector Location

Pin	Description	Pin	Description
1	ML_LANE0+	2	GND
3	ML_LANE0-	4	ML_LANE1+
5	GND	6	ML_LANE1-
7	ML_LANE2+	8	GND
9	ML_LANE2-	10	ML_LANE3+
11	GND	12	ML_LANE3-
13	AUX_CTRL_DET	14	GND
15	AUX_CTRL+	16	GND
17	AUX_CTRL-	18	HOT PLUG
19	GND	20	DP_PWR

Table 3-8: DisplayPort Connector Pinouts

3.2.8 EC Debug Connector

CN Label: **CN1**

CN Type: 18-pin header, p=2.00 mm

CN Location: See **Figure 3-9**

CN Pinouts: See **Table 3-9**

The EC debug connector is used for EC debug.

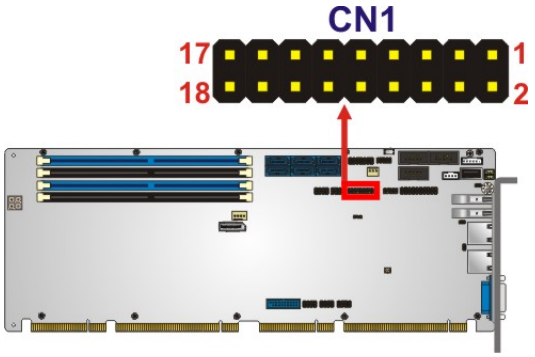


Figure 3-9: EC Debug Connector Location

Pin	Description	Pin	Description
1	EC_EPP_STB#	2	EC_EPP_AFD#
3	EC_EPP_PD0	4	NC
5	EC_EPP_PD1	6	EC_EPP_INIT#
7	EC_EPP_PD2	8	EC_EPP_SLIN#
9	EC_EPP_PD3	10	GND
11	EC_EPP_PD4	12	NC
13	EC_EPP_PD5	14	EC_EPP_BUSY
15	EC_EPP_PD6	16	EC_EPP_KSI5
17	EC_EPP_PD7	18	EC_EPP_KSI4

Table 3-9: EC Debug Connector Pinouts

3.2.9 Fan Connector (CPU)

CN Label:	**CPU_FAN1**
CN Type:	4-pin wafer, p=2.54 mm
CN Location:	See **Figure 3-10**
CN Pinouts:	See **Table 3-10**

The fan connector attaches to a CPU cooling fan.

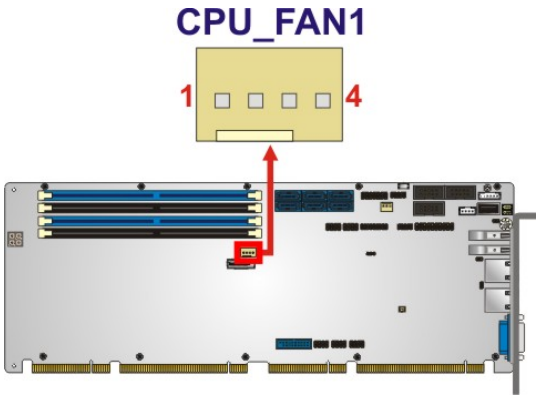


Figure 3-10: CPU Fan Connector Location

Pin	Description
1	GND
2	+12V
3	FANIO
4	PWM

Table 3-10: CPU Fan Connector Pinouts

3.2.10 Fan Connectors (System)

CN Label:	**SYS_FAN1**
CN Type:	3-pin wafer, p=2.54 mm
CN Location:	See **Figure 3-11**
CN Pinouts:	See **Table 3-11**

The fan connector attaches to a system cooling fan.

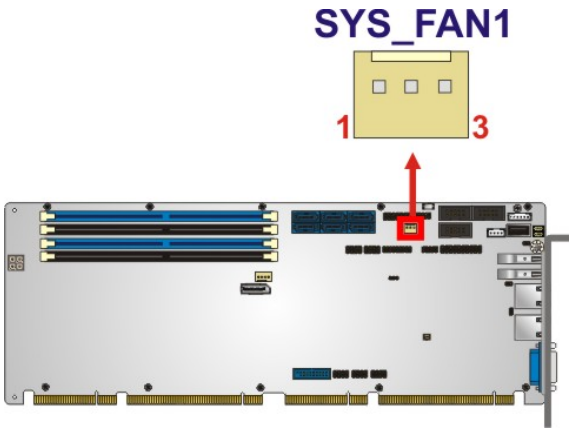


Figure 3-11: System Fan Connector Location

Pin	Description
1	FANIO
2	+12V (PWM)
3	GND

Table 3-11: System Fan (SYS_FAN1) Connector Pinouts

3.2.11 Front Panel Connector

CN Label: **F_PANEL1**

CN Type: 14-pin header, p=2.54 mm

CN Location: See **Figure 3-12**

CN Pinouts: See **Table 3-12**

The front panel connector connects to the indicator LEDs and buttons on the computer's front panel.

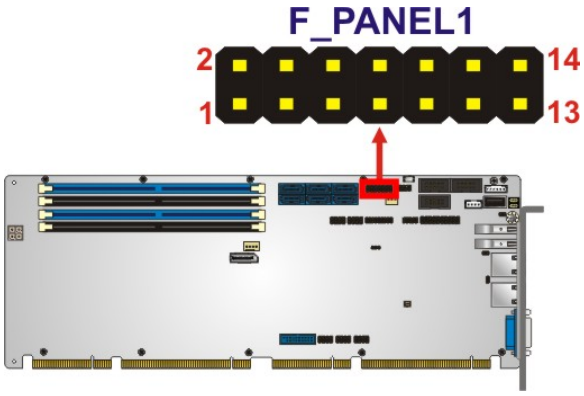


Figure 3-12: Front Panel Connector Location

Function	Pin	Description	Function	Pin	Description
Power LED	1	PWR_LED+	Speaker	2	SPKR+
	3	NC	IPMI LED	4	NC
	5	PWR_LED-		6	NC
Power Button	7	PWR_BTN+	Speaker	8	SPKR-
	9	PWR_BTN-		10	NC
HDD LED	11	HDD_LED+	Reset	12	Reset+
	13	HDD_LED-		14	Reset-

Table 3-12: Front Panel Connector Pinouts

3.2.12 I²C Connector

CN Label: **I2C1**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-13**

CN Pinouts: See **Table 3-13**

The I²C connector is used to connect I²C-bus devices to the motherboard.

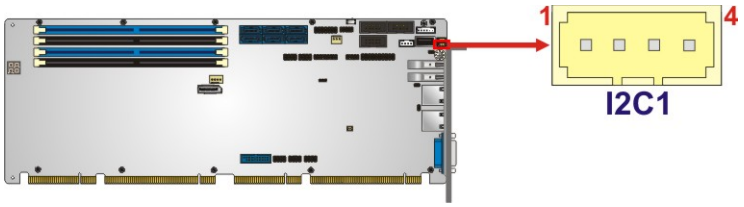


Figure 3-13: I²C Connector Location

Pin	Description
1	GND
2	I2C_DAT
3	I2C_CLK
4	+5V

Table 3-13: I²C Connector Pinouts

3.2.13 Keyboard and Mouse Connector

CN Label: **KB_MS1**

CN Type: 6-pin wafer, p=2.00 mm

CN Location: See **Figure 3-14**

CN Pinouts: See **Table 3-14**

The keyboard and mouse connector connects to a PS/2 Y-cable that can be connected to a PS/2 keyboard and mouse.

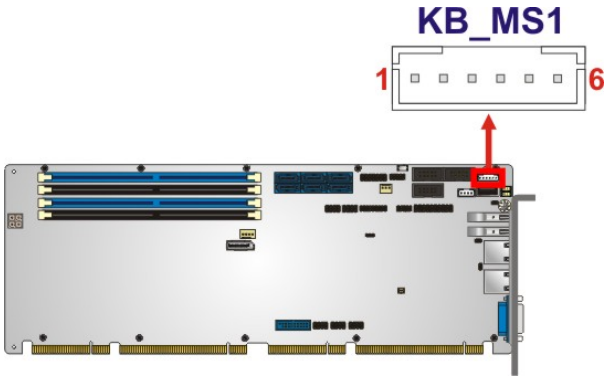


Figure 3-14: Keyboard and Mouse Connector Location

Pin	Description
1	VCC
2	Mouse Data
3	Mouse Clock
4	Keyboard Data
5	Keyboard Clock
6	GND

Table 3-14: Keyboard and Mouse Connector Pinouts

3.2.14 LAN LED Connectors

CN Label: **LED_LAN1, LED_LAN2**

CN Type: 2-pin header, p=2.54 mm

CN Location: See **Figure 3-15**

CN Pinouts: See **Table 3-15** and **Table 3-16**

The LAN LED connectors are used to connect to the LAN LED indicators on the chassis to indicate users the link activities of the two LAN ports.

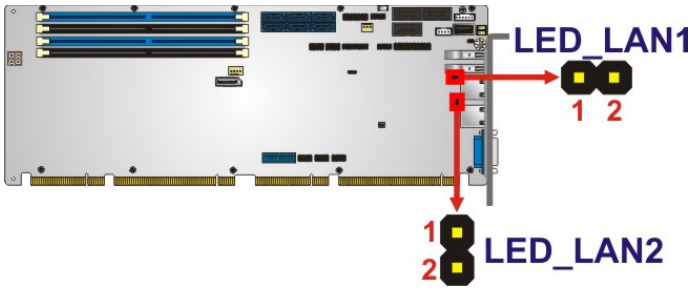


Figure 3-15: LAN LED Connector Locations

Pin	Description
1	+3.3V
2	LAN1_LED_LINK#_ACT

Table 3-15: LAN1 LED Connector (LED_LAN1) Pinouts

Pin	Description
1	+3.3V
2	LAN2_LED_LINK#_ACT

Table 3-16: LAN2 LED Connector (LED_LAN2) Pinouts

3.2.15 M.2 2280 Slot, M-Key

CN Label: **M2_M1**

CN Type: M.2 2280 M-key slot

CN Location: See **Figure 3-16**

CN Pinouts: See **Table 3-17**

The M.2 2280 slot is keyed in the M position. The M.2 slot supports PCIe x4 interfaces.

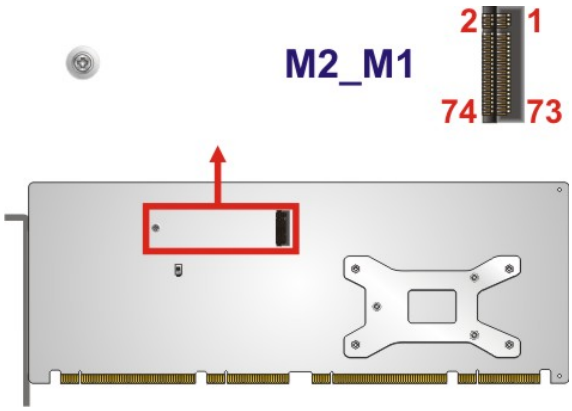


Figure 3-16: M.2 2280 Slot Location

Pin	Description	Pin	Description
1	GND	2	+3.3V
3	GND	4	+3.3V
5	PCIE_RXN3	6	N/C
7	PCIE_RXP3	8	N/C
9	GND	10	DAS/DSS#
11	PCIE_TXN3	12	+3.3V
13	PCIE_TXP3	14	+3.3V
15	GND	16	+3.3V
17	PCIE_RXN2	18	+3.3V
19	PCIE_RXP2	20	N/C
21	GND	22	N/C
23	PCIE_TXN2	24	N/C
25	PCIE_TXP2	26	N/C
27	GND	28	N/C
29	PCIE_RXN1	30	N/C
31	PCIE_RXP1	32	N/C
33	GND	34	N/C
35	PCIE_TXN1	36	N/C
37	PCIE_TXP1	38	DEVSLP
39	GND	40	N/C
41	PCIE_RXN0	42	N/C

Pin	Description	Pin	Description
43	PCIE_RXP0	44	N/C
45	GND	46	N/C
47	PCIE_TXN0	48	N/C
49	PCIE_TXP0	50	PERST#
51	GND	52	CLKREQ#
53	REFCLKN	54	PEWAKE
55	REFCLKP	56	N/C
57	GND	58	N/C
59	Notch	60	Notch
61	Notch	62	Notch
63	Notch	64	Notch
65	Notch	66	Notch
67	N/C	68	SUSCLK
69	PEDET	70	+3.3V
71	GND	72	+3.3V
73	GND	74	+3.3V
75	GND		

Table 3-17: M.2 2280 Connector Pinouts

3.2.16 Power Button

CN Label: **PWR_SW1**

CN Type: Push button

CN Location: See **Figure 3-17**

The on-board power button controls system power.

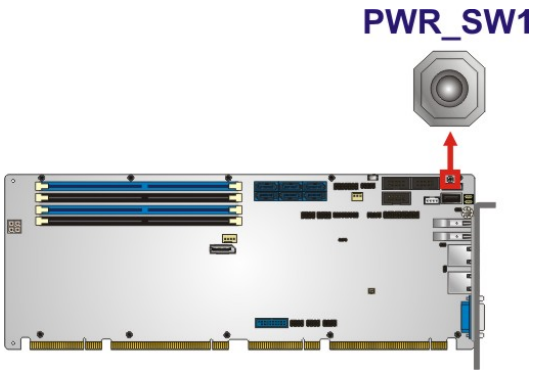


Figure 3-17: Power Button Location

3.2.17 RS-232 Serial Ports

CN Label: **COM1, COM2, COM3**

CN Type: 10-pin box header, p=2.54 mm

CN Location: See **Figure 3-18**

CN Pinouts: See **Table 3-18**

Each of these connectors provides RS-232 connections.

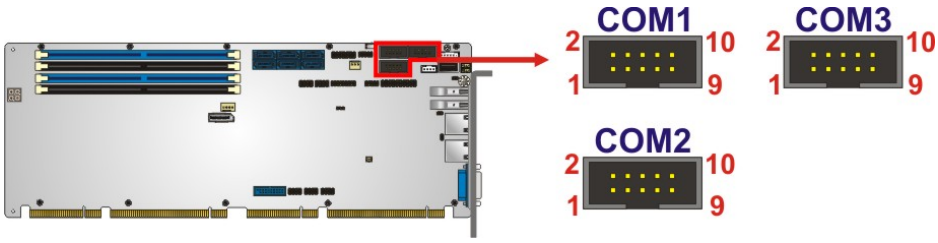


Figure 3-18: RS-232 Serial Port Locations

Pin	Description	Pin	Description
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI
9	GND	10	GND

Table 3-18: RS-232 Serial Port Pinouts

3.2.18 RS-422/485 Serial Port

CN Label:	**COM4**
CN Type:	4-pin wafer, p=2.00 mm
CN Location:	See **Figure 3-19**
CN Pinouts:	See **Table 3-19**

Each of these connectors provides RS-422/485 connections.

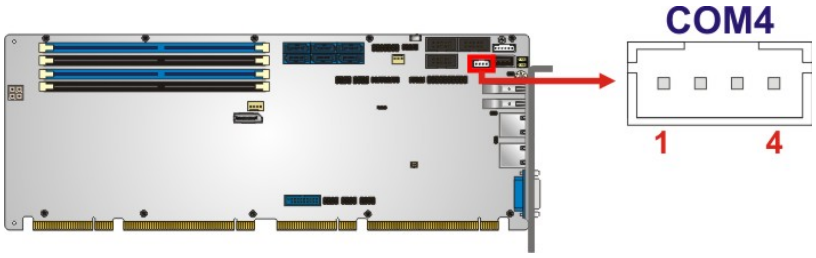


Figure 3-19: RS-422/485 Serial Port Locations

PIN NO.	DESCRIPTION
1	RXD422-
2	RXD422+
3	TXD422+/TXD485+
4	TXD422-/TXD485-

Table 3-19: RS-422/485 Serial Port Pinouts

Use the optional RS-422/485 cable to connect to a serial device. The pinouts of the D-sub 9 connector are listed below.

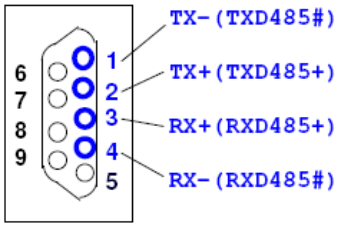
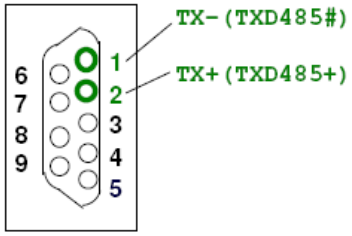
RS-422 Pinouts	RS-485 Pinouts
	

Table 3-20: DB-9 RS-422/485 Pinouts

3.2.19 SATA 6Gb/s Drive Connector

CN Label:	**S_ATA1, S_ATA2, S_ATA3, S_ATA4, S_ATA5, S_ATA6**
CN Type:	7-pin SATA drive connector
CN Location:	See **Figure 3-20**
CN Pinouts:	See **Table 3-21**

The SATA drive connectors can be connected to SATA drives and supports up to 6Gb/s data transfer rate.

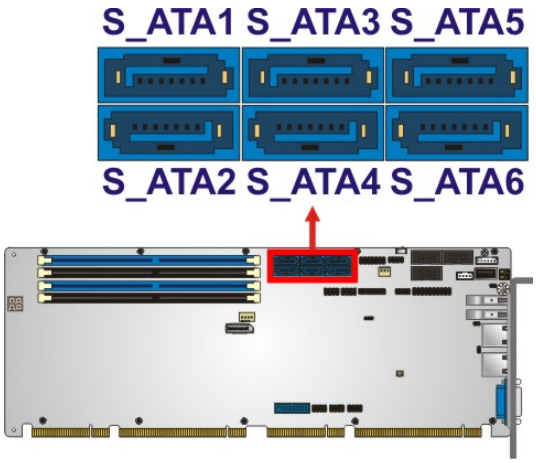


Figure 3-20: SATA 6Gb/s Drive Connector Locations

Pin	Description	Pin	Description
1	GND	2	TX+
3	TX-	4	GND
5	RX-	6	RX+
7	GND		

Table 3-21: SATA 6Gb/s Drive Connector Pinouts

3.2.20 SMBus Connector

CN Label: **SMB1**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-21**

CN Pinouts: See **Table 3-22**

The SMBus (System Management Bus) connector provides low-speed system management communications.

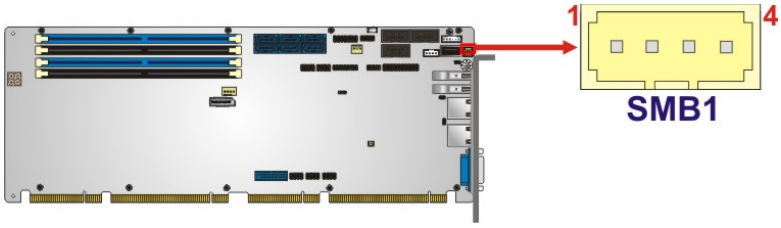


Figure 3-21: SMBus Connector Location

Pin	Description
1	GND
2	SMB_DATA
3	SMB_CLK
4	+5V

Table 3-22: SMBus Connector Pinouts

3.2.21 SPI Flash Connector

CN Label: **JSPI1**

CN Type: 8-pin header, p=2.54 mm

CN Location: See **Figure 3-22**

CN Pinouts: See **Table 3-23**

The SPI flash connector is used to flash the SPI ROM.

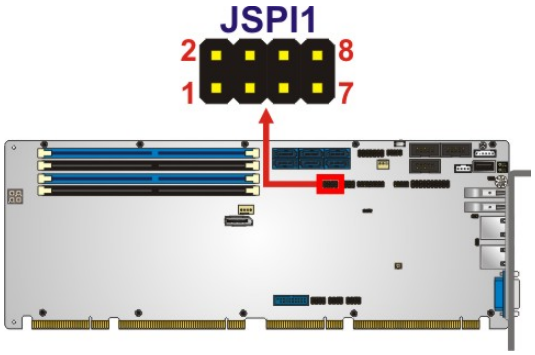


Figure 3-22: SPI Flash Connector Location

Pin	Description	Pin	Description
1	+3.3V	2	GND
3	SPI_CS	4	SPI_CLK_SW
5	SPI_SO_SW	6	SPI_SI_SW
7	NC	8	NC

Table 3-23: SPI Flash Connector Pinouts

3.2.22 SPI Flash Connector, EC

CN Label:	**JSPI2**
CN Type:	8-pin header, p=2.54 mm
CN Location:	See **Figure 3-23**
CN Pinouts:	See **Table 3-24**

The SPI flash connector is used to flash the EC ROM.

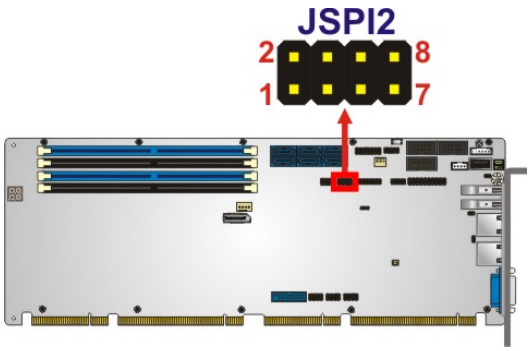


Figure 3-23: SPI EC Flash Connector Location

Pin	Description	Pin	Description
1	+3.3V	2	GND
3	SPI_CS_EC	4	SPI_CLK_EC
5	SPI_SO_EC	6	SPI_SI_EC
7	NC	8	NC

Table 3-24: SPI EC Flash Connector Pinouts

3.2.23 TPM Connector

CN Label: **TPM1**

CN Type: 20-pin header, p=2.54 mm

CN Location: See **Figure 3-24**

CN Pinouts: See **Table 3-25**

The TPM connector connects to a TPM module.

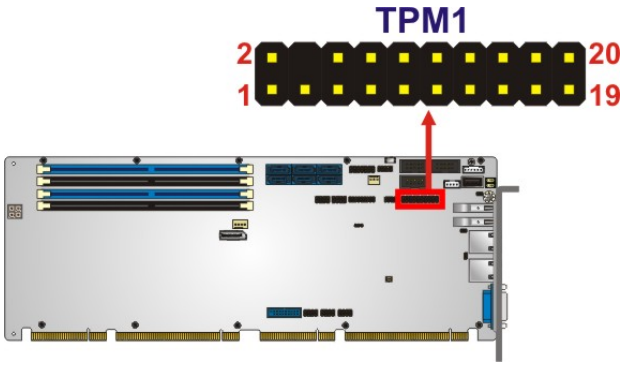


Figure 3-24: TPM Connector Location

Pin	Description	Pin	Description
1	LCLK	2	GND
3	LFRAME#	4	KEY
5	LRERST#	6	+5V
7	LAD3	8	LAD2
9	+3.3V	10	LAD1
11	LAD0	12	GND
13	SCL	14	SDA
15	SB3V	16	SERIRQ
17	GND	18	GLKRUN#
19	LPCPD#	20	LDRQ#

Table 3-25: TPM Connector Pinouts

3.2.24 USB 2.0 Connectors

CN Label:	**USB1, USB2, USB4**
CN Type:	8-pin header, p=2.54 mm
CN Location:	See **Figure 3-25**
CN Pinouts:	See **Table 3-26**

The USB 2.0 connectors connect to USB 2.0 devices. Each pin header provides two USB 2.0 ports.

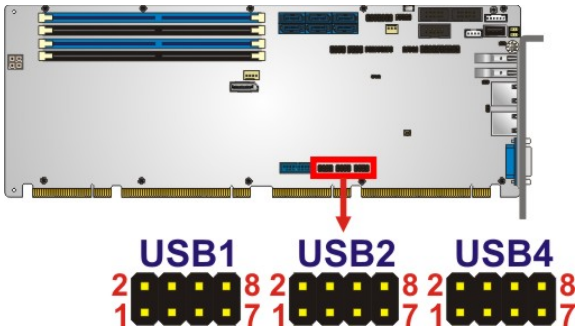


Figure 3-25: USB 2.0 Connector Locations

Pin	Description	Pin	Description
1	VCC	2	GND
3	USB_DATA-	4	USB_DATA+
5	USB_DATA+	6	USB_DATA-
7	GND	8	VCC

Table 3-26: USB 2.0 Connector Pinouts

3.2.25 USB 2.0 Connector (Type A)

CN Label: **USB3**

CN Type: USB Type A

CN Location: See **Figure 3-26**

CN Pinouts: See **Table 3-27**

The USB Type A connector connects to a USB 2.0/1.1 device.

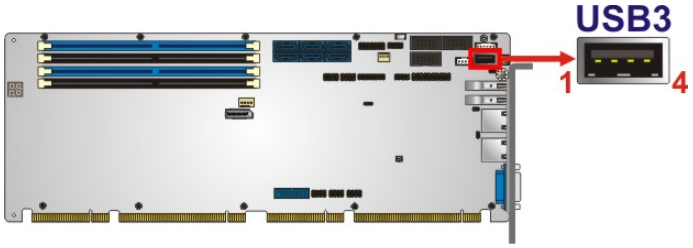


Figure 3-26: USB 2.0 Connector (Type A) Pinout Location

Pin	Description
1	VCC
2	DATA-
3	DATA+
4	GROUND

Table 3-27: USB 2.0 Connector (Type A) Pinouts

3.2.26 USB 3.1 Gen 1 Connector

CN Label: **USB3-1**

CN Type: 19-pin box header, p=2.00 mm

CN Location: See **Figure 3-27**

CN Pinouts: See **Table 3-28**

The USB 3.1 Gen 1 (5 Gb/s) connector connects to USB 3.1 Gen 1 devices. This connector provides two USB 3.1 Gen 1 ports.

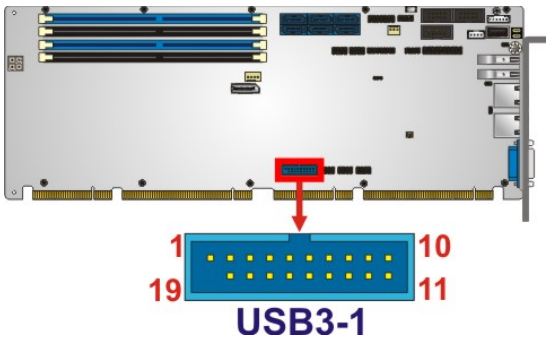


Figure 3-27: USB 3.1 Gen 1 Connector Location

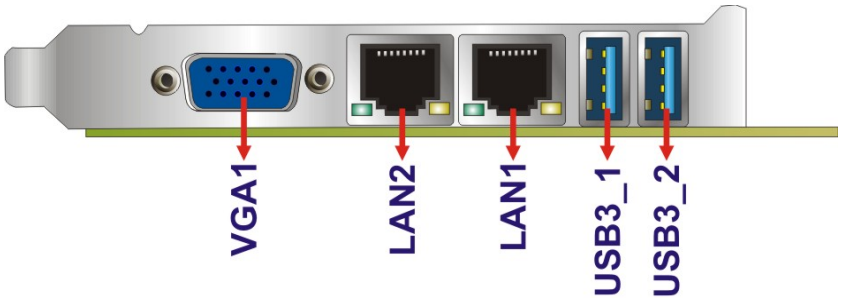
Pin	Description	Pin	Description
1	VCC	11	USB_DATA+
2	USB3_RX-	12	USB_DATA-
3	USB3_RX+	13	GND
4	GND	14	USB3_TX+
5	USB3_TX-	15	USB3_TX-
6	USB3_TX+	16	GND
7	GND	17	USB3_RX+
8	USB_DATA-	18	USB3_RX-
9	USB_DATA+	19	VCC
10	NC		

Table 3-28: USB 3.1 Gen 1 Connector Pinouts

3.3 External Peripheral Interface Connector Panel

The figures below show the external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

PCIE-Q370



PCIE-Q370-HDMI

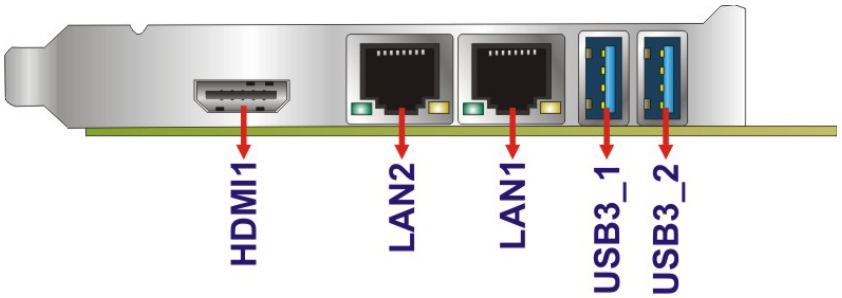


Figure 3-28: External Peripheral Interface Connector

3.3.1 Ethernet Connectors

CN Label: **LAN1, LAN2**

CN Type: RJ-45

CN Location: See **Figure 3-28**

CN Pinouts: See **Table 3-29**

Each LAN connector connects to a local network.

Pin	Description	Pin	Description
1	LAN_MDI0P	5	LAN_MDI2P
2	LAN_MDI0N	6	LAN_MDI2N
3	LAN_MDI1P	7	LAN_MDI3P
4	LAN_MDI1N	8	LAN_MDI3N

Table 3-29: LAN Pinouts

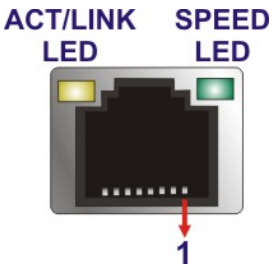


Figure 3-29: Ethernet Connector

3.3.2 USB 3.1 Gen 1 Connectors

CN Label: **USB3_1, USB3_2**

CN Type: USB 3.1

CN Location: See **Figure 3-28**

CN Pinouts: See **Table 3-30**

There are two external USB 3.1 Gen 1 (5 Gb/s) connectors on the PCIE-Q370.

Pin	Description	Pin	Description
1	VBUS	2	D-
3	D+	4	GND
5	STDA_SSRX_N	6	STDA_SSRX_P
7	GND_DRAIN	8	STDA_SSTX_N
9	STDA_SSTX_P		

Table 3-30: USB 3.1 Gen 1 Port Pinouts

3.3.3 VGA Connector (Standard SKU Only)

CN Label: **VGA1**

CN Type: 15-pin VGA

CN Location: See **Figure 3-28**

CN Pinouts: See **Table 3-31**

The 15-pin VGA connector connects to a monitor that accepts a standard VGA input.

NOTE:

The VGA port is only available on the PCIE-Q370 SKU.

The user has to connect the VGA connector to the monitor before system booting as the VGA output function is supported via the eDP to VGA converter.

Pin	Description	Pin	Description
1	RED	2	GREEN
3	BLUE	4	NC
5	GND	6	HOT PLUG DETECT
7	GND	8	GND
9	VCC	10	GND
11	NC	12	DDCDA
13	HSYNC	14	VSYNC
15	DDCCLK		

Table 3-31: VGA Connector Pinouts

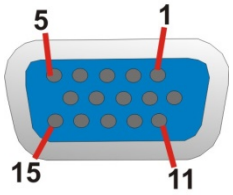


Figure 3-30: VGA Connector

3.3.4 HDMI Connector (HDMI SKU Only)

CN Label: **HDMI1**

CN Type: 23-pin HDMI port

CN Location: See **Figure 3-28**

CN Pinouts: See **Table 3-32**

The HDMI connector can connect to an HDMI device.

NOTE:

The HDMI port is only available on the PCIE-Q370-HDMI SKU.

Pin	Description	Pin	Description
1	HDMI_DATA2	2	GND
3	HDMI_DATA2#	4	HDMI_DATA1
5	GND	6	HDMI_DATA1#
7	HDMI_DATA0	8	GND
9	HDMI_DATA0#	10	HDMI_CLK
11	GND	12	HDMI_CLK#
13	N/C	14	N/C
15	HDMI_SCL	16	HDMI_SDA
17	GND	18	+5V
19	HDMI_HPD	20	HDMI_GND
21	HDMI_GND	22	HDMI_GND
23	HDMI_GND		

Table 3-32: HDMI Connector Pinouts

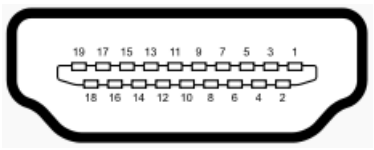


Figure 3-31: HDMI Connector

Chapter

4

Installation

4.1 Anti-static Precautions

WARNING:

Failure to take ESD precautions during the installation of the PCIE-Q370 may result in permanent damage to the PCIE-Q370 and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the PCIE-Q370. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the PCIE-Q370 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband***: - Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding***:- Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad***: When configuring the PCIE-Q370, place it on an anti-static pad. This reduces the possibility of ESD damaging the PCIE-Q370.
- ***Only handle the edges of the PCB***:-: When handling the PCB, hold the PCB by the edges.

4.2 Installation Considerations

NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

WARNING:

The installation instructions described in this manual should be carefully followed in order to prevent damage to the components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  - The user manual provides a complete description of the PCIE-Q370 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the PCIE-Q370 on an anti-static pad:
  - When installing or configuring the motherboard, place it on an anti-static pad. This helps to prevent potential ESD damage.
- Turn all power to the PCIE-Q370 off:
  - When working with the PCIE-Q370, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the PCIE-Q370, **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.3 Socket LGA1151 CPU Installation

WARNING:

CPUs are expensive and sensitive components. When installing the CPU please be careful not to damage it in anyway. Make sure the CPU is installed properly and ensure the correct cooling kit is properly installed.

DO NOT touch the pins at the bottom of the CPU. When handling the CPU, only hold it on the sides.

To install the CPU, follow the steps below.

Step 1: **Disengage the load lever** by pressing the lever down and slightly outward to clear the retention tab. Fully open the lever. See **Figure 4-1**.

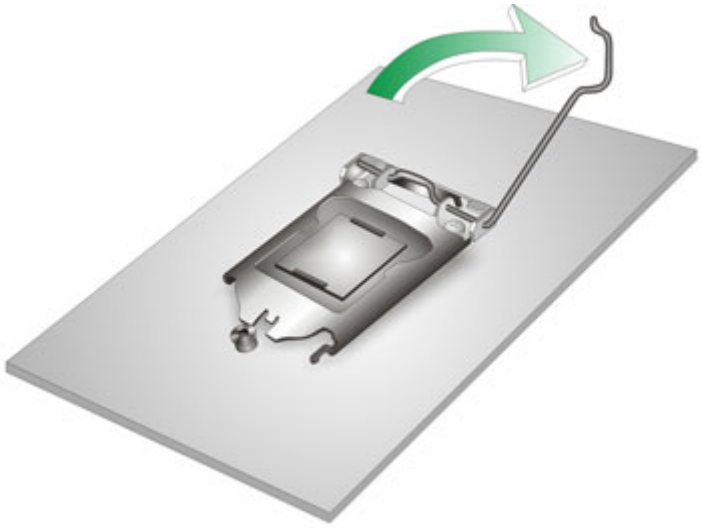


Figure 4-1: Disengage the CPU Socket Load Lever

Step 2: **Open the socket and remove the protective cover.** The black protective cover can be removed by pulling up on the tab labeled "Remove". See **Figure 4-2**.

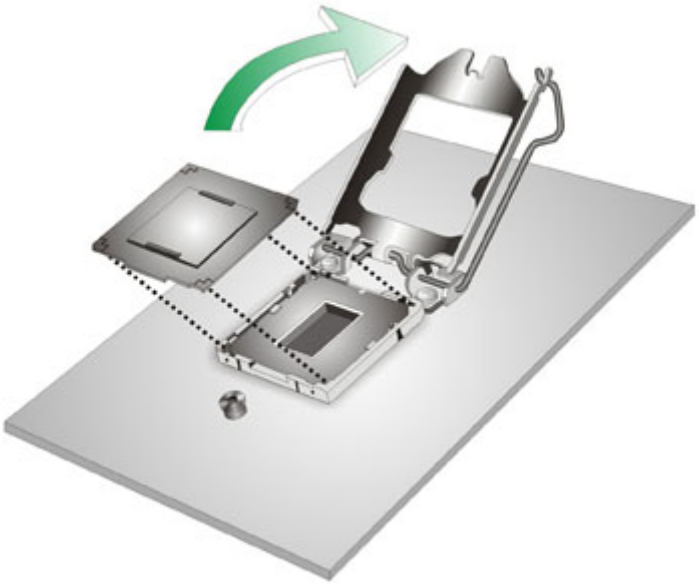


Figure 4-2: Remove Protective Cover

Step 3: **Inspect the CPU socket.** Make sure there are no bent pins and make sure the socket contacts are free of foreign material. If any debris is found, remove it with compressed air.

Step 4: **Orientate the CPU properly.** The contact array should be facing the CPU socket.

WARNING:

DO NOT touch the pins at the bottom of the CPU. When handling the CPU, only hold it on the sides.

Step 5: **Correctly position the CPU.** Match the Pin 1 mark with the cut edge on the CPU socket.

Step 6: **Align the CPU pins.** Locate pin 1 and the two orientation notches on the CPU. Carefully match the two orientation notches on the CPU with the socket alignment keys.

Step 7: **Insert the CPU.** Gently insert the CPU into the socket. If the CPU pins are properly aligned, the CPU should slide into the CPU socket smoothly. See **Figure 4-3**.

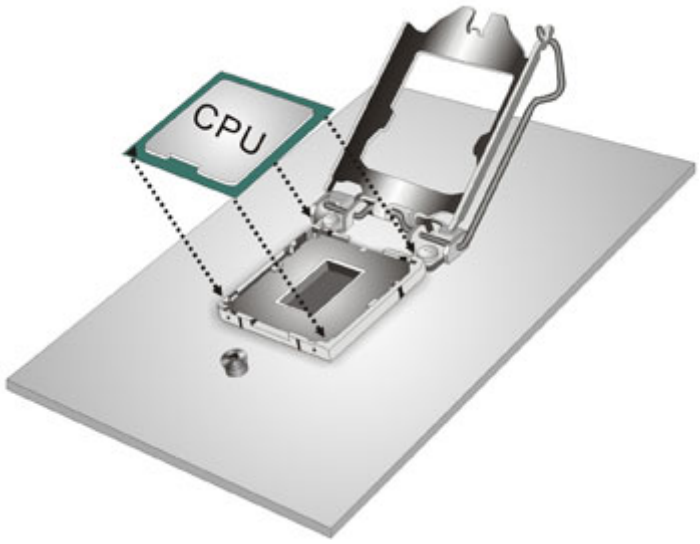


Figure 4-3: Insert the Socket LGA1151 CPU

Step 8: **Close the CPU socket.** Close the load plate and pull the load lever back a little to have the load plate be able to secure to the knob. Engage the load lever by pushing it back to its original position (**Figure 4-4**). There will be some resistance, but will not require extreme pressure.

Figure 4-4: Close the Socket LGA1151

Step 9: **Connect the 12 V power to the board.** Connect the 12 V power from the power supply to the board.

4.4 Socket LGA1151 Cooling Kit Installation

WARNING:

DO NOT attempt to install a push-pin cooling fan.

The pre-installed support bracket prevents the board from bending and is ONLY compatible with captive screw type cooling fans.

The cooling kit can be bought from IEI. The cooling kit has a heat sink and fan.

WARNING:

Do not wipe off (accidentally or otherwise) the pre-sprayed layer of thermal paste on the bottom of the heat sink. The thermal paste between the CPU and the heat sink is important for optimum heat dissipation.

To install the cooling kit, follow the instructions below.

Step 1: A cooling kit bracket is pre-installed on the rear of the motherboard. See **Figure 4-5.**

Figure 4-5: Cooling Kit Support Bracket

Step 2: **Place the cooling kit onto the socket LGA1151 CPU**. Make sure the CPU cable can be properly routed when the cooling kit is installed.

Step 3: **Mount the cooling kit**. Gently place the cooling kit on top of the CPU. Make sure the four threaded screws on the corners of the cooling kit properly pass through the holes of the cooling kit bracket.

Step 4: **Tighten the screws**. Use a screwdriver to tighten the four screws. In a diagonal pattern, tighten each screw a few turns then move to the next one, until they are all secured. Do not overtighten the screws.

Step 5: **Connect the fan cable**. Connect the cooling kit fan cable to the CPU fan connector on the PCIE-Q370. Carefully route the cable and avoid heat generating chips and fan blades.

4.5 DIMM Installation

To install a DIMM, please follow the steps below and refer to **Figure 4-6**.

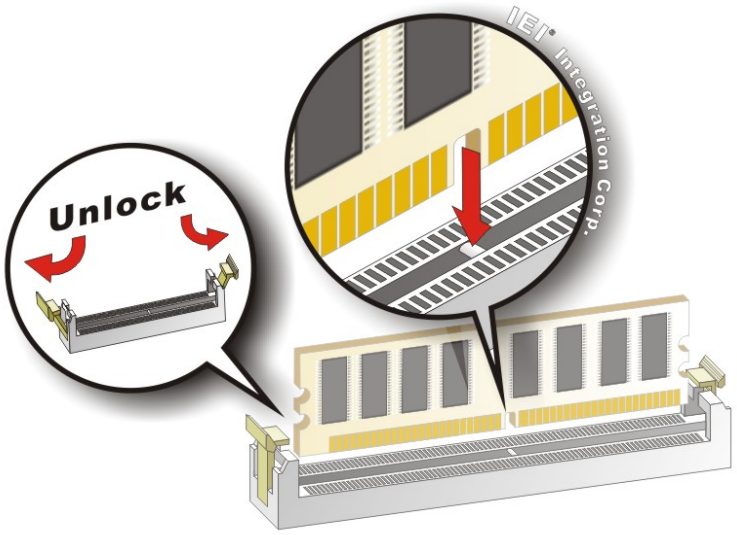


Figure 4-6: DIMM Installation

Step 1: **Open the DIMM socket handles**. Open the two handles outwards as far as they can. See **Figure 4-6**.

Step 2: **Align the DIMM with the socket**. Align the DIMM so the notch on the memory lines up with the notch on the memory socket. See **Figure 4-6**.

Step 3: **Insert the DIMM**. Once aligned, press down until the DIMM is properly seated. Clip the two handles into place. See **Figure 4-6**.

Step 4: **Removing a DIMM**. To remove a DIMM, push both handles outward. The memory module is ejected by a mechanism in the socket.

CAUTION:

For quad channel configuration, install four identical memory modules that feature the same capacity, timings, voltage, number of ranks and the same brand.

4.6 System Configuration

The system configuration should be performed before installation.

4.6.1 AT/ATX Power Mode Setting

The AT and ATX power mode selection is made through the AT/ATX power mode switch which is shown in **Figure 4-7**.

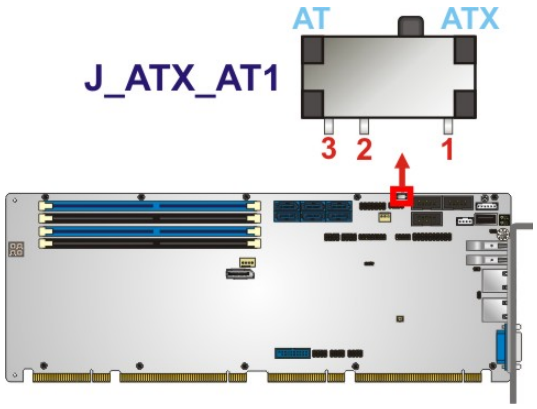


Figure 4-7: AT/ATX Power Mode Switch Location

Setting	Description
1-2 (right)	ATX power mode (default)
2-3 (left)	AT power mode

Table 4-1: AT/ATX Power Mode Switch Settings

4.6.2 Clear CMOS Button

To reset the BIOS, remove the on-board battery and press the clear CMOS button for three seconds or more. The clear CMOS button location is shown in **Figure 4-8**.

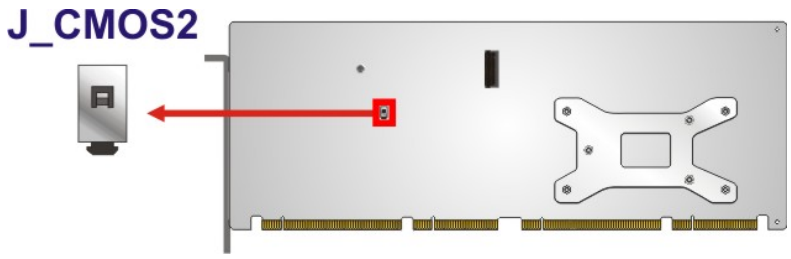


Figure 4-8: Clear CMOS Button Location

4.6.3 PCIe x16 Channel Mode Setup

The PCIE-Q370 supports one PCIe x16 interface on the backplane. The PCIe x16 channel mode setup is made through the BIOS menu in "Chipset → System Agent (SA) Configuration → PEG Port Configuration". Use the **PEG Link Width Configuration** BIOS option to configure the PCIe x16 channel mode.

Options	Description
1x16	Sets the PCIe x16 link width as one PCIe x16 slot (default)
2x8	Sets the PCIe x16 link width as two PCIe x8 slots
1x8, 2x4	Sets the PCIe x16 link width as one PCIe x8 and two PCIe x4

Table 4-2: PCIe x16 Channel Mode Setup

Please refer to **Section 5.4.1.3** for detailed information.

4.6.4 Flash Descriptor Security Override Jumper

The flash descriptor security override jumper (J_FLASH1) allows to enable or disable the ME firmware update. Refer to **Table 4-3** and **Figure 4-9** for the jumper location and settings.

Setting	Description
Short 1-2	Disabled (default)
Short 2-3	Enabled

Table 4-3: Flash Descriptor Security Override Jumper Settings

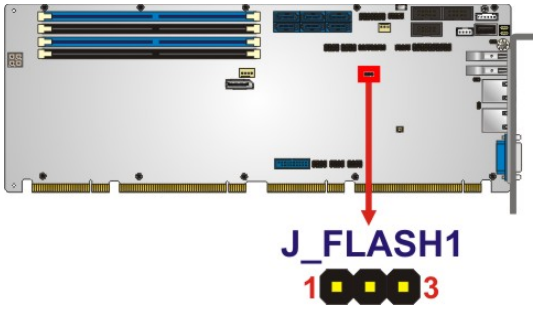


Figure 4-9: Flash Descriptor Security Override Jumper Location

To update the ME firmware, please follow the steps below.

Step 1: Before turning on the system power, short pin 2-3 of the flash descriptor security override jumper.

Step 2: Update the BIOS and ME firmware, and then turn off the system power.

Step 3: Remove the metal clip on the flash descriptor security override jumper or return to its default setting (short pin 1-2).

Step 4: Restart the system. The system will reboot 2 ~ 3 times to complete the ME firmware update.

4.6.5 USB Power Selection

The USB power selection is made through the BIOS menu in "Chipset → PCH-IO Configuration". Use the **USB Power SW1** and the **USB Power SW2** BIOS options to configure whether to provide power to the corresponding USB connectors when the system is in S3/S4 sleep state. See **Table 4-4** and refer to **Table 4-5** to select the USB power source. These options are valid only when the above **Power Saving Function (ERP)** BIOS option is disabled.

BIOS Options	Configured USB Ports
USB Power SW1	USB3_1 (external USB 3.1 Gen 1 port) USB3_2 (external USB 3.1 Gen 1 port) USB3 (internal USB 2.0 port, Type A)
USB Power SW2	USB1 (internal USB 2.0 ports) USB2 (internal USB 2.0 ports) USB4 (internal USB 2.0 ports) USB3-1 (internal USB 3.1 Gen 1 ports)

Table 4-4: BIOS Options and Configured USB Ports

Options	Description
+5V DUAL	+5V dual (default)
+5V	+5V

Table 4-5: USB Power Source Setup

Please refer to **Section 5.4.2** for BIOS setup.

4.7 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the onboard connectors.

4.7.1 SATA Drive Connection

The PCIE-Q370 is shipped with one SATA drive cable. To connect the SATA drives to the connectors, please follow the steps below.

Step 1: **Locate the connectors**. The locations of the SATA drive connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Insert the cable connector into the on-board SATA drive connector until it clips into place. See **Figure 4-10**.

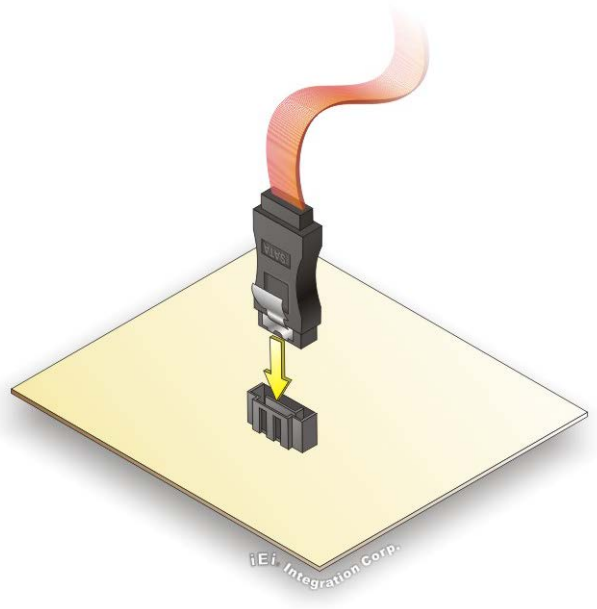


Figure 4-10: SATA Drive Cable Connection

Step 3: **Connect the cable to the SATA disk**. Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 4-11**.

Step 4: **Connect the SATA power cable**. Connect the SATA power connector to the back of the SATA drive. See **Figure 4-11**.

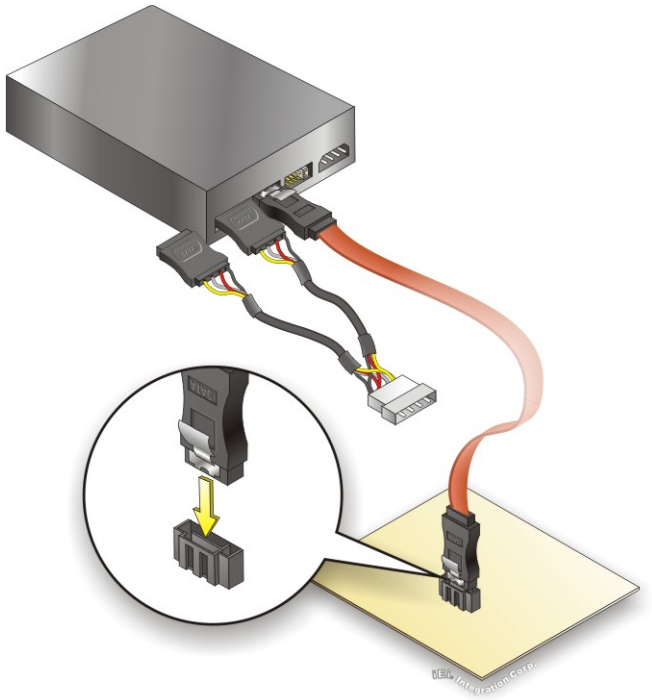


Figure 4-11: SATA Power Drive Connection

The SATA power cable can be bought from IEI. See Optional Items in Section 2.4.

4.8 Software Installation

All the drivers for the PCIE-Q370 are available on IEI Resource Download Center (https://download.ieiworld.com). Type PCIE-Q370 and press Enter to find all the relevant software, utilities, and documentation.

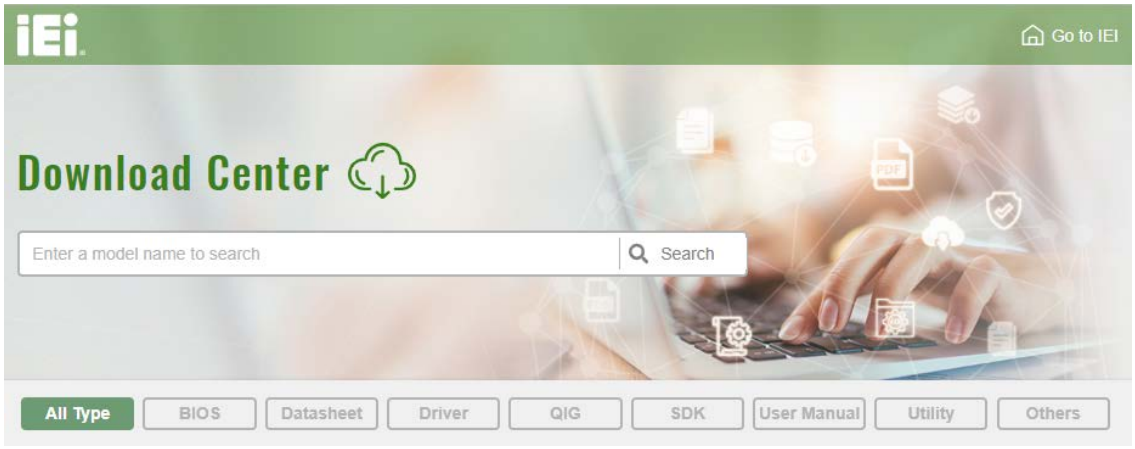
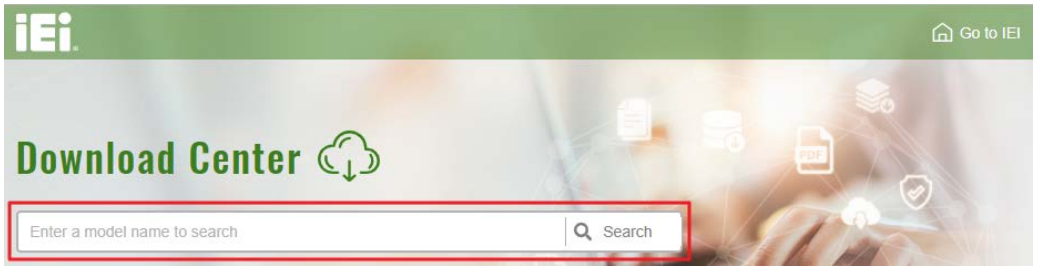


Figure 4-12: IEI Resource Download Center

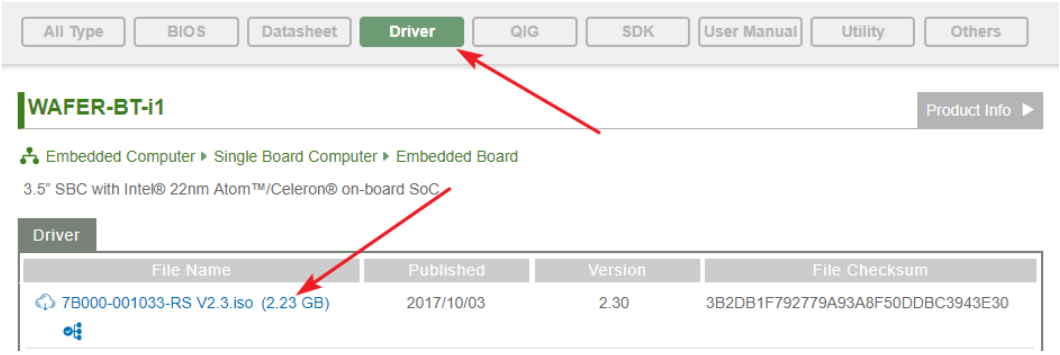
4.8.1 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

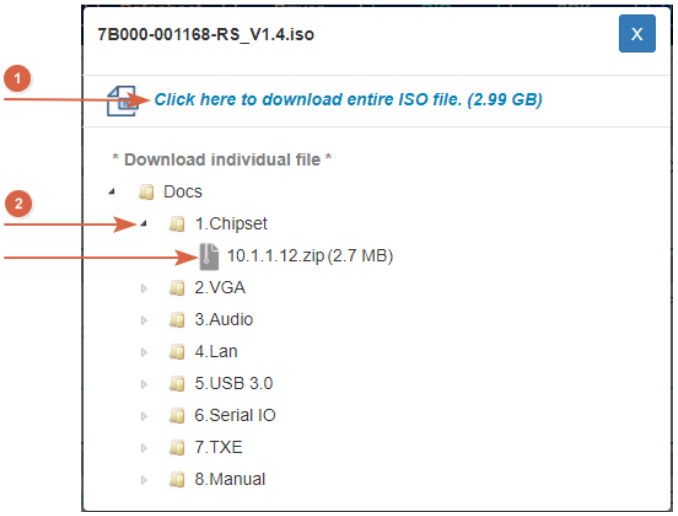
Step 1: Go to https://download.ieiworld.com. Type PCIE-Q370 and press Enter.



Step 2: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.



Step 3: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or click the small arrow to find an individual driver and click the file name to download (❷).



NOTE:

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content. On Windows 7 system, an additional tool (such as Virtual CD-ROM Control Panel from Microsoft) is needed to mount the file.

4.9 Intel® AMT Setup Procedure

The PCIE-Q370 is featured with the Intel® Active Management Technology (AMT). To enable the Intel® AMT function, follow the steps below.

Step 1: Make sure at least one of the memory sockets is installed with a DDR4 DIMM.

Step 2: Connect an Ethernet cable to the RJ-45 connector labeled **LAN1**.

Step 3: The AMI BIOS options regarding the Intel® ME or Intel® AMT must be enabled,

Step 4: Properly install the Intel® Management Engine Components drivers from the iAMT Driver & Utility directory in the driver CD.

Step 5: Configure the Intel® Management Engine BIOS extension (MEBx). To get into the Intel® MEBx settings, press <Ctrl+P> after a single beep during boot-up process. Enter the Intel® current ME password as it requires (the Intel® default password is **admin**).

NOTE:

To change the password, enter a new password following the strong password rule (containing at least one upper case letter, one lower case letter, one digit and one special character, and be at least eight characters).

Chapter

5

BIOS

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.

NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the **DEL** or **F2** key as soon as the system is turned on or
2. Press the **DEL** or **F2** key when the "**Press DEL or F2 to enter SETUP**" message appears on the screen.

If the message disappears before the **DEL or F2** key is pressed, restart the computer and try again.

5.1.2 Using Setup

Use the arrow keys to highlight items, press **ENTER** to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press **ESC** to quit. Navigation keys are shown in the following table.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes
-	Decrease the numeric value or make changes
Page Up	Move to the previous page
Page Dn	Move to the next page

Key	Function
Esc	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Load previous values
F3	Load optimized defaults
F4	Save changes and Exit BIOS

Table 5-1: BIOS Navigation Keys

5.1.3 Getting Help

When **F1** is pressed, a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press **Esc**.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the clear CMOS button described in **Chapter 4**.

5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

5.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered.

The **Main** menu gives an overview of the basic system information.

BIOS Menu 1: Main

The **Main** menu has two user configurable fields:

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

➔ **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:

WARNING!

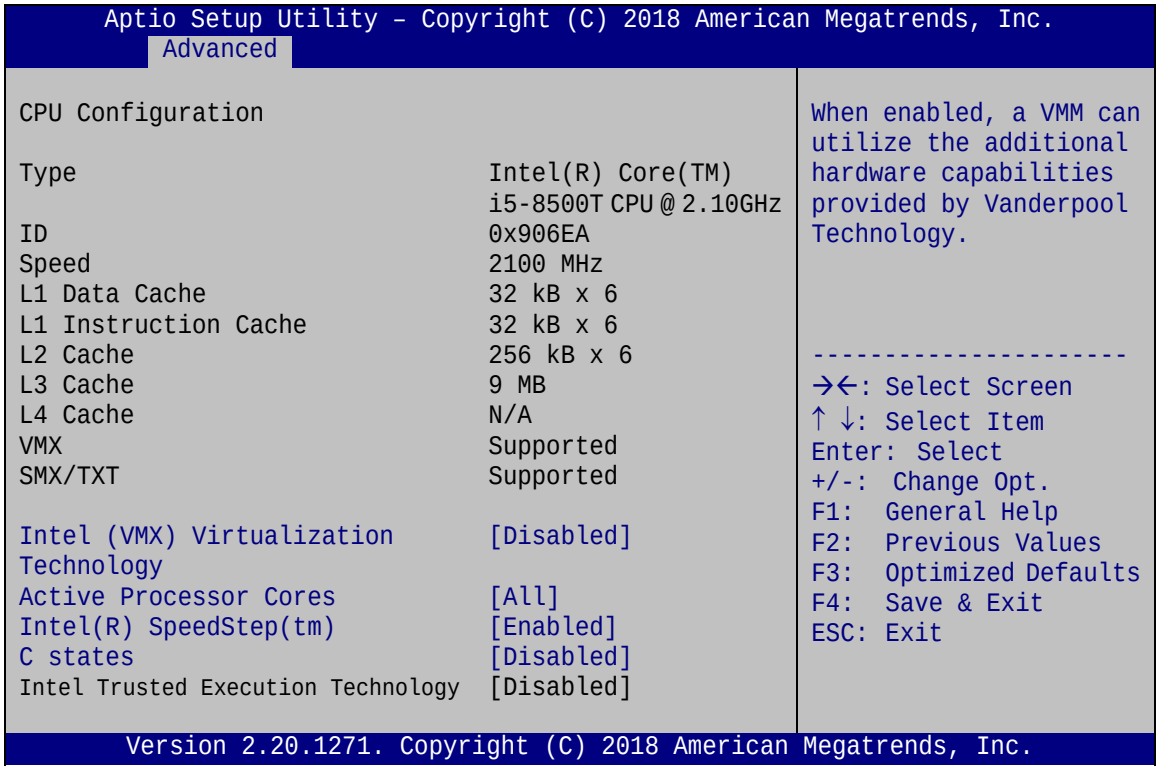
Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.

```
      Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
  Main    Advanced  Chipset  Security    Boot    Save & Exit

> CPU Configuration                          Trusted Computing
> PCH-FW Configuration                       Settings
> Trusted Computing
> ACPI Settings                              ----------------------
> iWDD H/M Monitor                           →←: Select Screen
> F81866 Super IO Configuration              ↑ ↓: Select Item
> RTC Wake Settings                          Enter:  Select
> Serial Port Console Redirection            +/-:  Change Opt.
> USB Configuration                          F1:  General Help
> CSM Configuration                          F2:  Previous Values
> NVMe Configuration                         F3:  Optimized Defaults
> iEi Feature                                F4:  Save & Exit
                                             ESC:  Exit
      Version 2.20.1271. Copyright (C) 2018 American Megatrends, Inc.
```

BIOS Menu 2: Advanced

5.3.1 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 3**) to view detailed CPU specifications or enable the Intel Virtualization Technology.



BIOS Menu 3: CPU Configuration

➔ **Intel (VMX) Virtualization Technology [Disabled]**

Use the **Intel (VMX) Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

➔	**Disabled**	**DEFAULT**	Disables Intel Virtualization Technology.
➔	**Enabled**		Enables Intel Virtualization Technology.

➔ **Active Processor Cores [All]**

Use the **Active Processor Cores** BIOS option to enable numbers of cores in the processor package.

➔	**All**	**DEFAULT**	Enable all cores in the processor package.
➔	**1**		Enable one core in the processor package.
➔	**2**		Enable two cores in the processor package.
➔	**3**		Enable three cores in the processor package.
➔	**4**		Enable four cores in the processor package.
➔	**5**		Enable five cores in the processor package.

➔ **Intel(R) SpeedStep(tm) [Enabled]**

Use the **Intel(R) SpeedStep(tm)** option to enable or disable the Intel® SpeedStep Technology which allows more than two frequency ranges to be supported.

➔	**Disabled**		Disables Intel® SpeedStep Technology
➔	**Enabled**	**DEFAULT**	Enables Intel® SpeedStep Technology

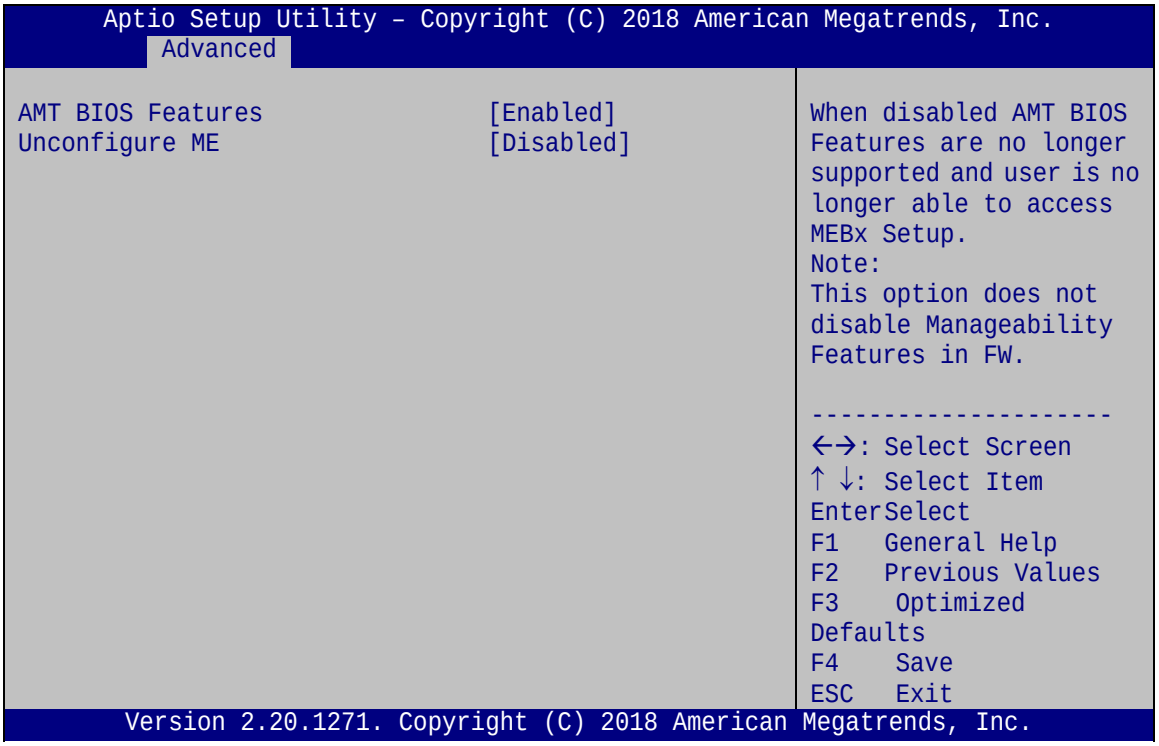
➔ **C states [Disabled]**

Use the **C states** option to enable or disable CPU power management which allows CPU to go to C states when it is not 100% utilized.

➔	**Disabled**	**DEFAULT**	Disables CPU power management
➔	**Enabled**		Enables CPU power management

5.3.2 PCH-FW Configuration

The **PCH-FW Configuration** menu (**BIOS Menu 4**) allows Intel® Active Management Technology (AMT) options to be configured.



BIOS Menu 4: PCH-FW Configuration

➔ **AMT BIOS Features [Enabled]**

Use the **AMT BIOS Features** option to enable or disable the access to MEBx setup.

➔ **Disabled** Disable access to MEBx setup.

➔ **Enabled** **DEFAULT** Enable access to MEBx setup.

➔ **Unconfigure ME [Disabled]**

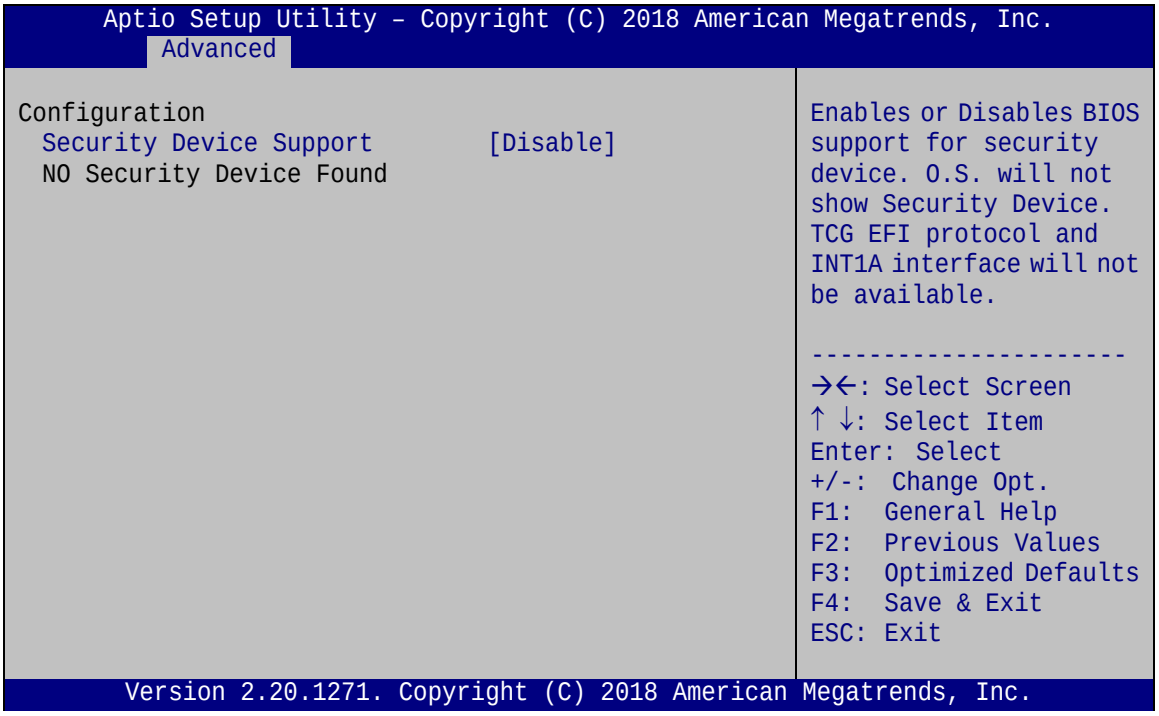
Use the **Unconfigure ME** option to unconfigure ME with resetting MEBx password to default.

➔ **Disabled** **DEFAULT** Not unconfigure ME with resetting MEBx password to default

➔ **Enabled** Unconfigure ME with resetting MEBx password to default

5.3.3 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 5**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).



BIOS Menu 5: Trusted Computing

➔ **Security Device Support [Disable]**

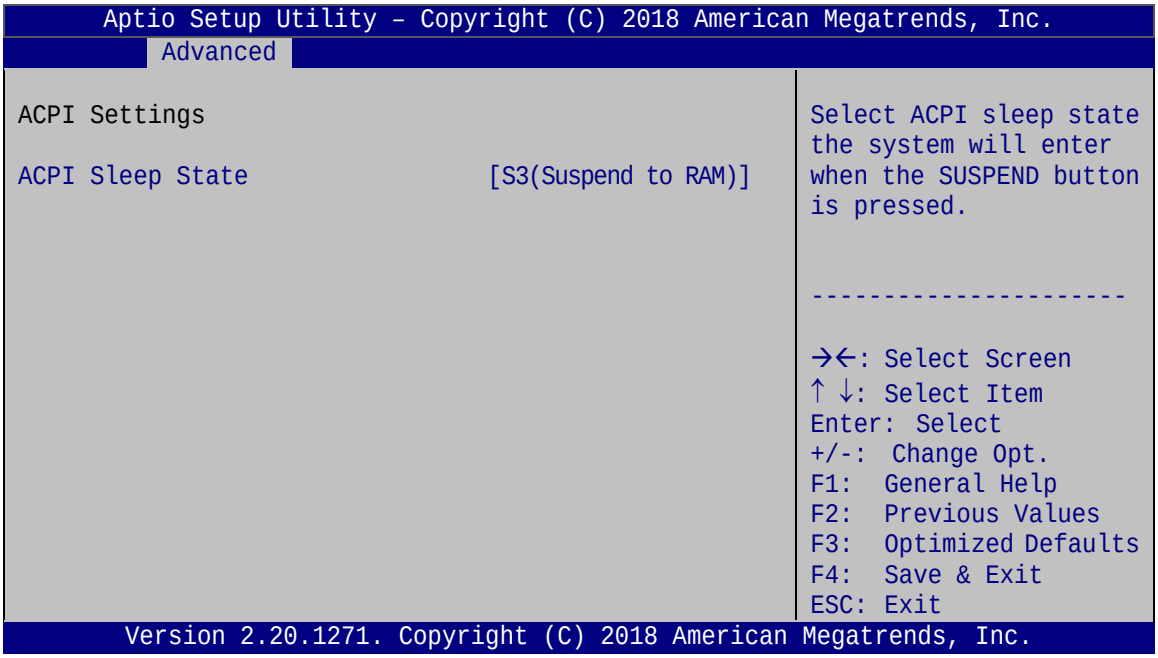
Use the **Security Device Support** option to configure support for the TPM.

➔ **Disable** **DEFAULT** TPM support is disabled.

➔ **Enable** TPM support is enabled.

5.3.4 ACPI Settings

The **ACPI Settings** menu (**BIOS Menu 6**) configures the Advanced Configuration and Power Interface (ACPI) options.



BIOS Menu 6: ACPI Settings

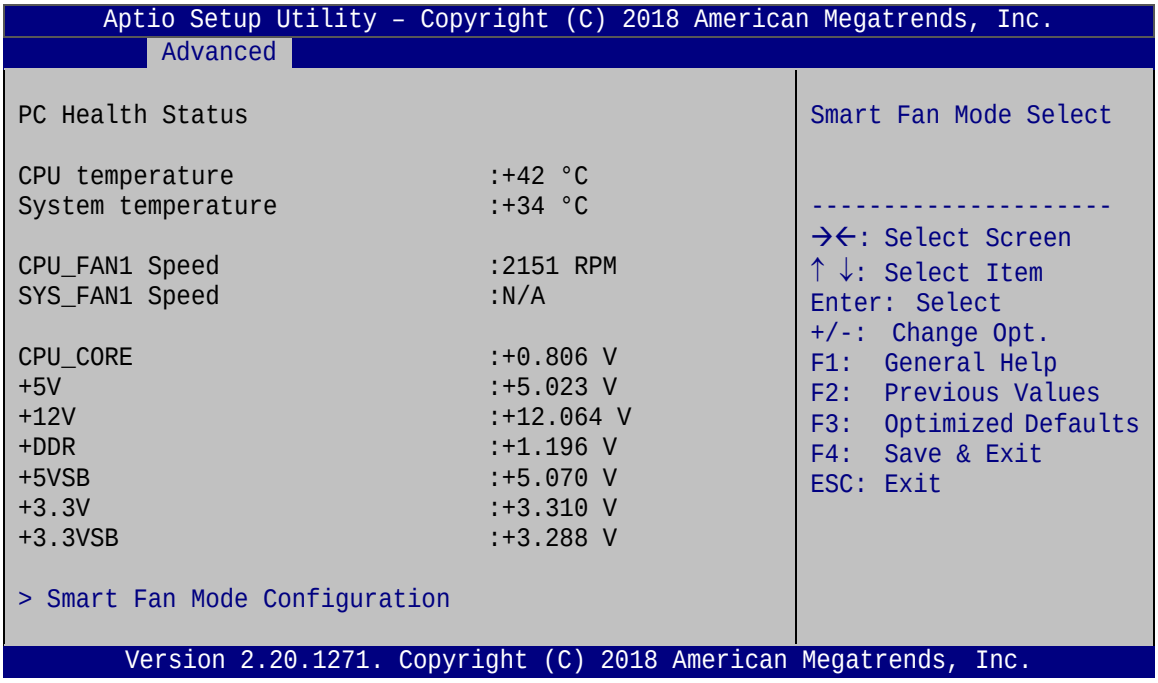
➔ **ACPI Sleep State [S3 (Suspend to RAM)]**

Use the **ACPI Sleep State** option to specify the sleep state the system enters when it is not being used.

➔ **S3 (Suspend to RAM)**	**DEFAULT**	The caches are flushed and the CPU is powered off. Power to the RAM is maintained. The computer returns slower to a working state, but more power is saved.

5.3.5 iWDD H/W Monitor

The **iWDD H/W Monitor** menu (**BIOS Menu 7**) contains the fan configuration submenu, and displays the system temperature and CPU fan speed.



BIOS Menu 7: iWDD H/W Monitor

➔ **PC Health Status**

The following system parameters and values are shown. The system parameters that are monitored are:

- System Temperatures:
  - CPU Temperature
  - System Temperature
- Fan Speeds:
  - CPU Fan Speed
  - System Fan Speed
- Voltages:
  - CPU_CORE
  - +5V

- +12V
- DDR
- +5VSB
- +3.3V
- +3.3VSB

5.3.5.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 8**) to configure the CPU/system fan temperature and speed settings.

```
Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
        Advanced
Smart Fan Mode Configuration                    Smart Fan Mode Select

CPU_FAN1 Smart Fan Control        [Auto Mode]
Auto mode fan start temperature   50
Auto mode fan off temperature     40
Auto mode fan start PWM           30
Auto mode fan slope PWM           2

SYS_FAN1 Smart Fan Control        [Auto Mode]
Auto mode fan start temperature   50
Auto mode fan off temperature     40
Auto mode fan start PWM           30
Auto mode fan slope PWM           1

                                  ---------------------
                                  →←: Select Screen
                                  ↑ ↓: Select Item
                                  Enter:  Select
                                  +/-:  Change Opt.
                                  F1:   General Help
                                  F2:   Previous Values
                                  F3:   Optimized Defaults
                                  F4:   Save & Exit
                                  ESC:  Exit
Version 2.20.1271. Copyright (C) 2018 American Megatrends, Inc.
```

BIOS Menu 8: Smart Fan Mode Configuration

➔ **CPU_FAN1 Smart Fan Control/SYS_FAN1 Smart Fan Control [Auto Mode]**

Use the **CPU_FAN1 Smart Fan Control/SYS_FAN1 Smart Fan Control** option to configure the CPU/System Smart Fan.

➔ **Manual Mode**		The fan spins at the speed set in Manual Mode settings.
➔ **Auto Mode**	**DEFAULT**	The fan adjusts its speed using Auto Mode settings.

The following options can only be set if the CPU/SYS Smart Fan Control option is set to Auto Mode.

➔ **Auto mode fan start temperature**

If the CPU temperature is between **fan off** and **fan start**, the fan speed change to **fan start PWM**. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **Auto mode fan off temperature**

If the CPU temperature is lower than the value set this option, the fan speed change to be lowest. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **Auto mode fan start PWM**

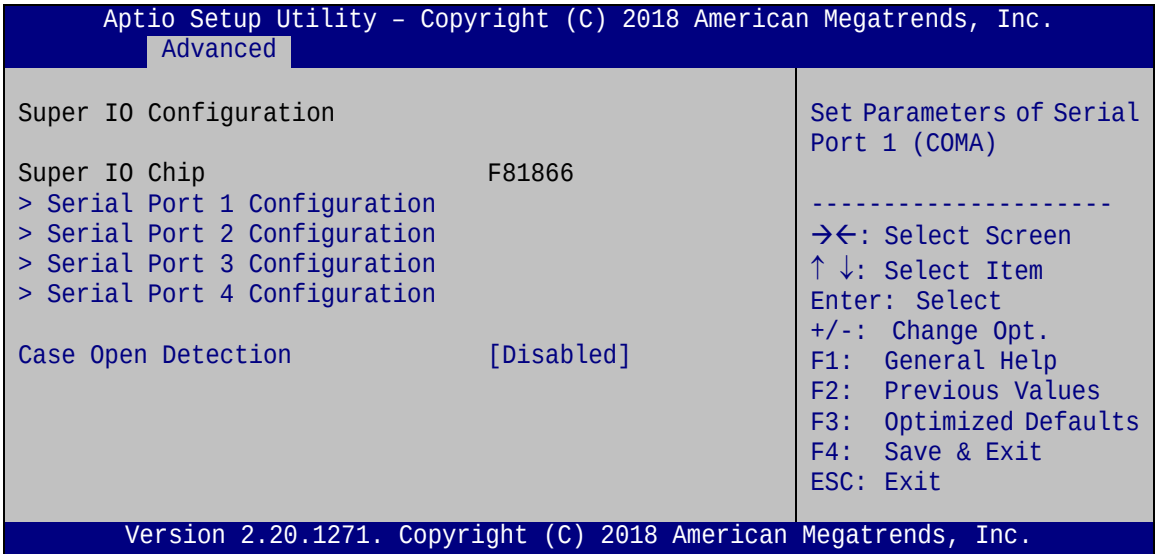
Use the **Auto mode fan start PWM** option to set the PWM start value. Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **Auto mode fan slope PWM**

Use the **Auto mode fan slope PWM** option to select the linear rate at which the PWM mode increases with respect to an increase in temperature. Use the + or – key to change the value or enter a decimal number between 1 and 8.

5.3.6 F81866 Super IO Configuration

Use the **F81866 Super IO Configuration** menu (**BIOS Menu 9**) to set or change the configurations for the parallel ports and serial ports.



BIOS Menu 9: F81866 Super IO Configuration

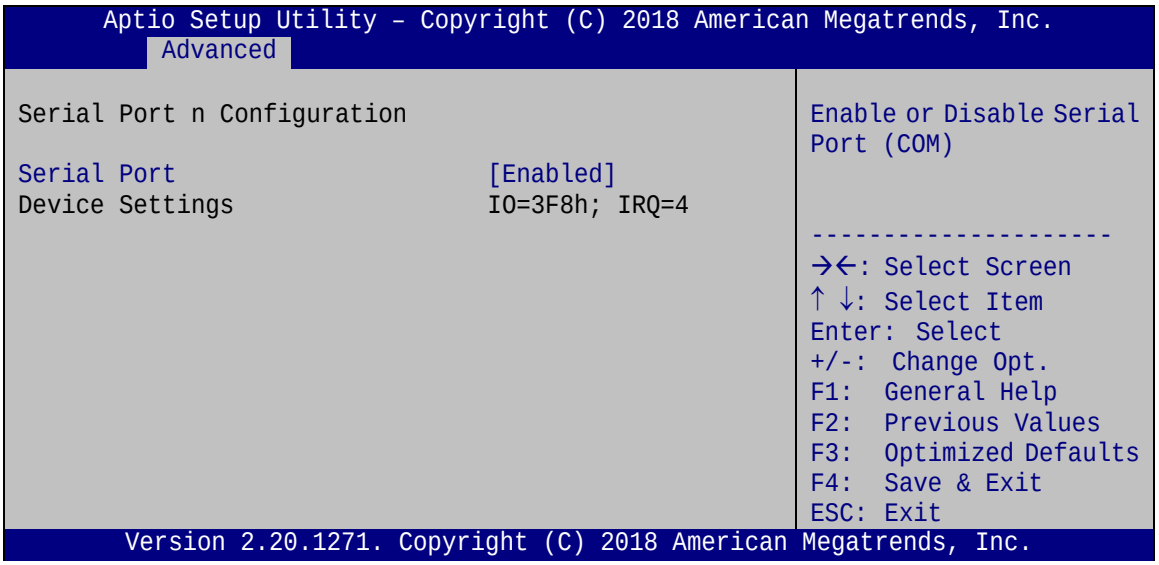
➔ **Case Open Beep [Disabled]**

Use the **Case Open Beep** option to enable or disable the case open beep function.

➔	**Disabled**	**DEFAULT**	Disable the case open beep function
➔	**Enabled**		Enable the case open beep function

5.3.6.1 Serial Port 1 Configuration

Use the **Serial Port 1 Configuration** menu (**BIOS Menu 10**) to configure the serial port n.



BIOS Menu 10: Serial Port 1 Configuration Menu

➔ **Serial Port [Enabled]**

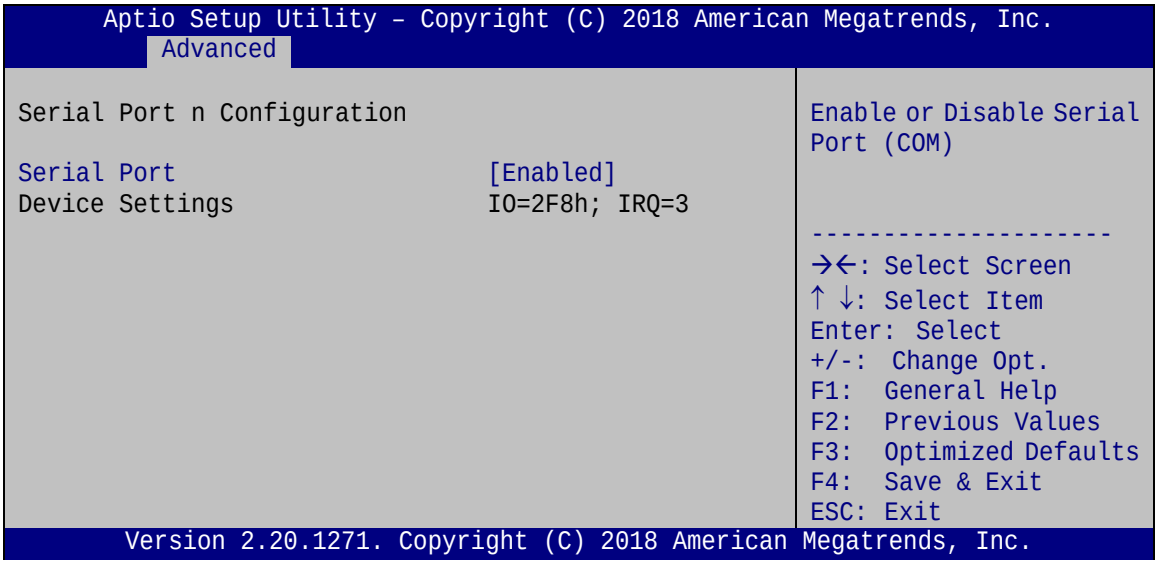
Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled** Disable the serial port

➔ **Enabled** **DEFAULT** Enable the serial port

5.3.6.2 Serial Port 2 Configuration

Use the **Serial Port 2 Configuration** menu (BIOS Menu 11: Serial Port 2 Configuration Menu**BIOS Menu 11**) to configure the serial port n.



BIOS Menu 11: Serial Port 2 Configuration Menu

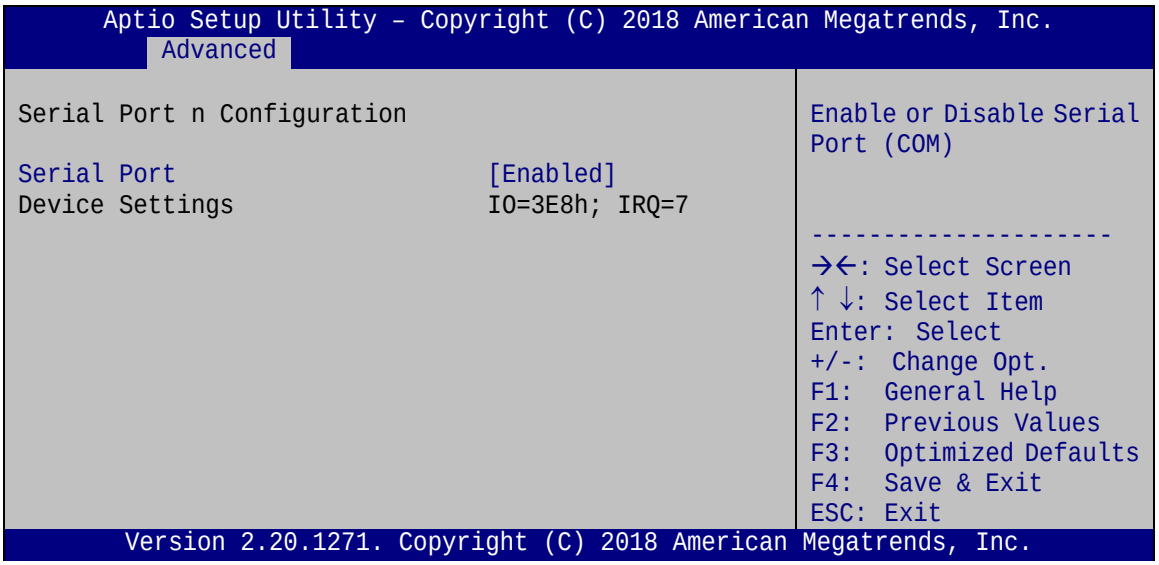
➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔	**Disabled**		Disable the serial port
➔	**Enabled**	**DEFAULT**	Enable the serial port

5.3.6.3 Serial Port 3 Configuration

Use the **Serial Port 3 Configuration** menu (**BIOS Menu 12**) to configure the serial port n.



BIOS Menu 12: Serial Port 3 Configuration Menu

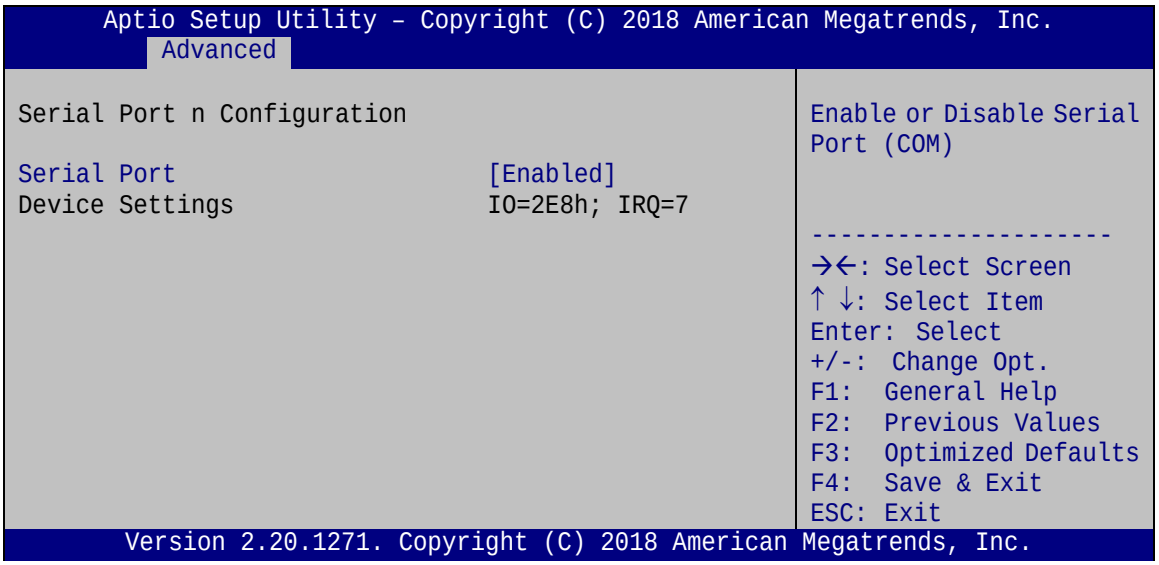
➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled** Disable the serial port
- ➔ **Enabled** **DEFAULT** Enable the serial port

5.3.6.4 Serial Port 4 Configuration

Use the **Serial Port 4 Configuration** menu (**BIOS Menu 13**) to configure the serial port n.



BIOS Menu 13: Serial Port 4 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled** Disable the serial port
- ➔ **Enabled** **DEFAULT** Enable the serial port

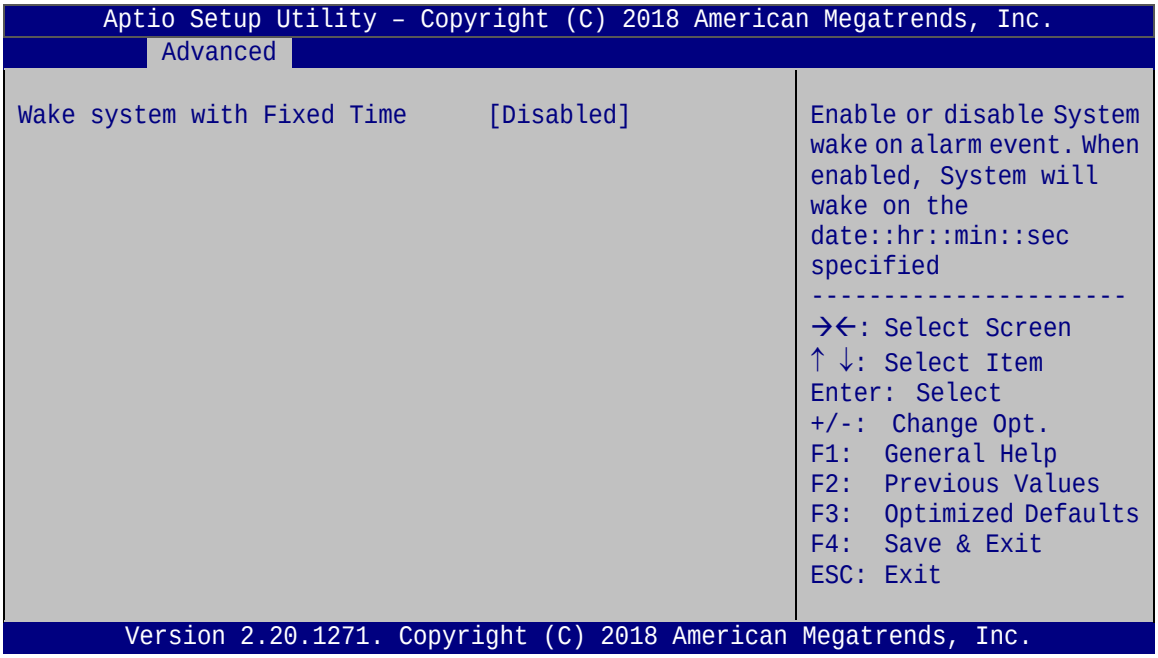
➔ **Transfer Mode [RS485]**

Use the **Transfer Mode** option to select the Serial Port 4 signaling mode.

- ➔ **RS485** **DEFAULT** Serial Port 4 signaling mode is RS-485

5.3.7 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 14**) enables the system to wake at the specified time.



BIOS Menu 14: RTC Wake Settings

➔ **Wake system with Fixed Time [Disabled]**

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

➔ **Disabled** **DEFAULT** The real time clock (RTC) cannot generate a wake event

➔ **Enabled** If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be selected:

Wake up date

Wake up hour

Wake up minute

Wake up second

After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

5.3.8 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 15**) allows the console redirection options to be configured. Console redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.

```
      Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
          Advanced
 COM1                                                  | Console Redirection
 Console Redirection            [Disabled]             | Enable or Disable
> Console Redirection Settings
 COM2
 Console Redirection            [Disabled]
> Console Redirection Settings
 COM3
 Console Redirection            [Disabled]
> Console Redirection Settings
 COM4
 Console Redirection            [Disabled]
> Console Redirection Settings                        | ----------------------
                                                      | →←: Select Screen
 iAMT SOL                                             | ↑ ↓: Select Item
                                                      | Enter: Select
 COM5 (Pci Bus0,Dev0,Func0) (Disabled)                | +/-: Change Opt.
 Console Redirection            Port Is Disabled      | F1: General Help
                                                      | F2: Previous Values
 Legacy Console Redirection                           | F3: Optimized Defaults
> Legacy Console Redirection Settings                 | F4: Save & Exit
                                                      | ESC: Exit
      Version 2.20.1271. Copyright (C) 2018 American Megatrends, Inc.
```

BIOS Menu 15: Serial Port Console Redirection

➔ **Console Redirection [Disabled]**

Use **Console Redirection** option to enable or disable the console redirection function.

➔ **Disabled**	**DEFAULT**	Disabled the console redirection function
➔ **Enabled**		Enabled the console redirection function

The following options are available in the **Console Redirection Settings** submenu when the **Console Redirection** option is enabled.

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** option to specify the remote terminal type.

➔ **VT100**		The target terminal type is VT100
➔ **VT100+**		The target terminal type is VT100+
➔ **VT-UTF8**		The target terminal type is VT-UTF8
➔ **ANSI**	**DEFAULT**	The target terminal type is ANSI

➔ **Bits per second [115200]**

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match the other side. Long or noisy lines may require lower speeds.

➔ **9600**		Sets the serial port transmission speed at 9600.
➔ **19200**		Sets the serial port transmission speed at 19200.
➔ **57600**		Sets the serial port transmission speed at 57600.
➔ **115200**	**DEFAULT**	Sets the serial port transmission speed at 115200.

➔ **Data Bits [8]**

Use the **Data Bits** option to specify the number of data bits.

➔ **7**		Sets the data bits at 7.
➔ **8**	**DEFAULT**	Sets the data bits at 8.

➔ **Parity [None]**

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

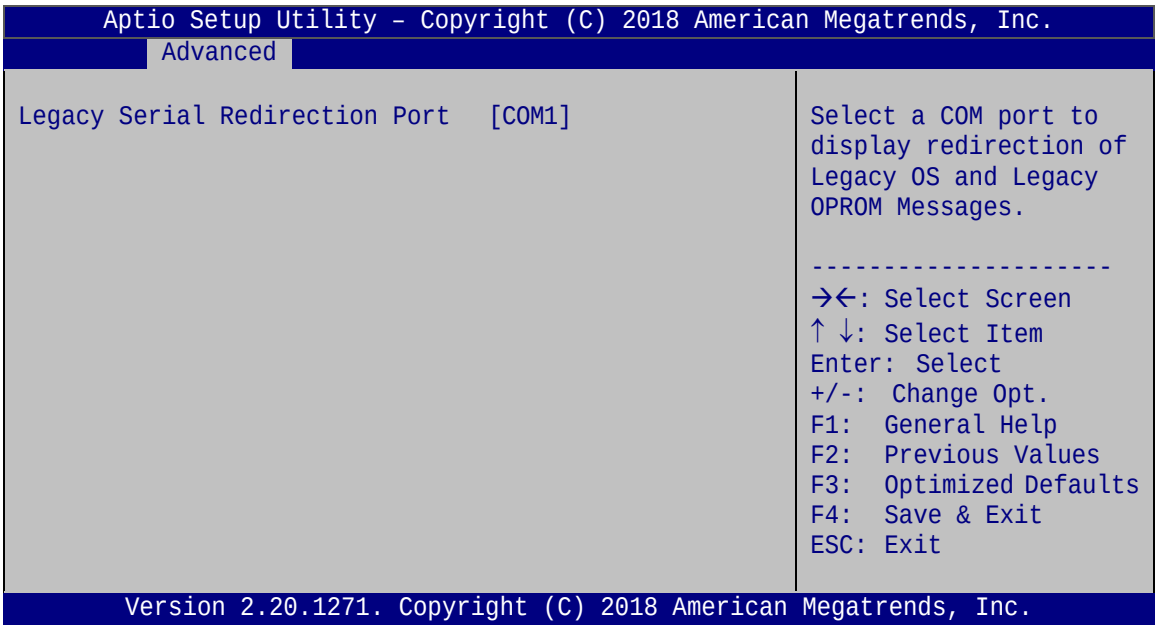
➔ **None**	**DEFAULT**	No parity bit is sent with the data bits.
➔ **Even**		The parity bit is 0 if the number of ones in the data bits is even.
➔ **Odd**		The parity bit is 0 if the number of ones in the data bits is odd.
➔ **Mark**		The parity bit is always 1. This option does not provide error detection.
➔ **Space**		The parity bit is always 0. This option does not provide error detection.

➔ **Stop Bits [1]**

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

➔ **1**	**DEFAULT**	Sets the number of stop bits at 1.
➔ **2**		Sets the number of stop bits at 2.

5.3.8.1 Legacy Console Redirection Settings



BIOS Menu 16: Legacy Console Redirection Settings

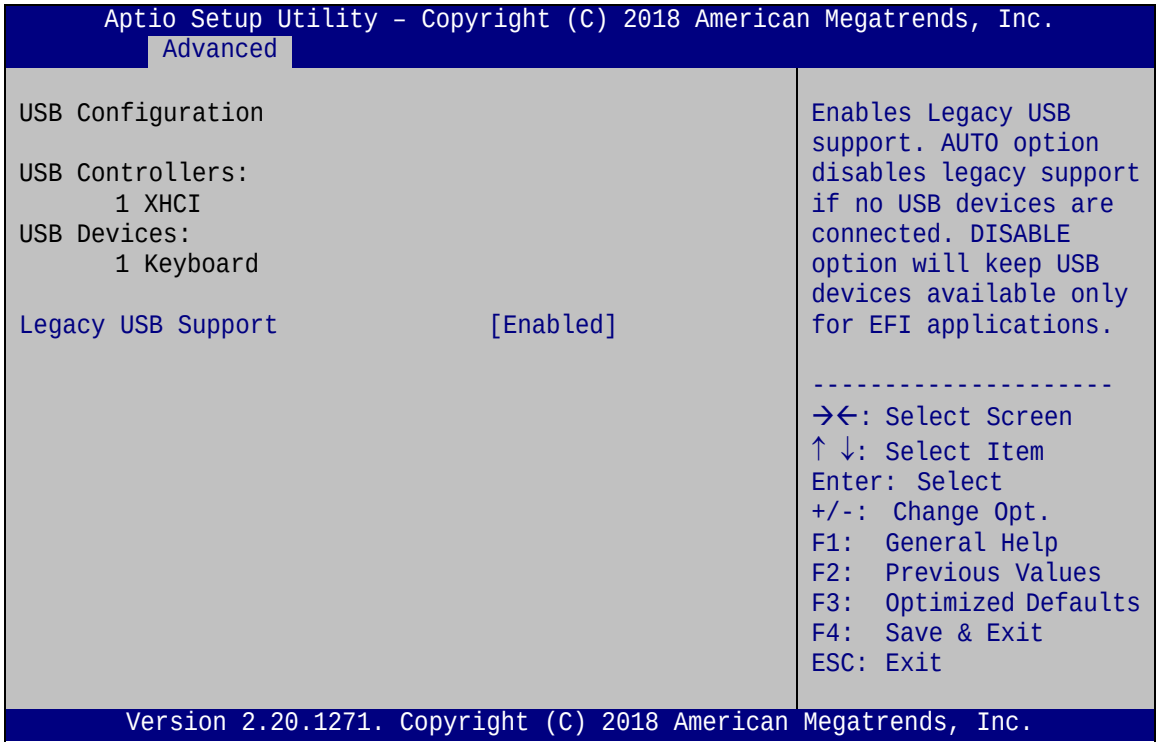
➔ **Legacy Serial Redirection Port [COM1]**

Use the **Legacy Serial Redirection Port** option to select a COM port to display redirection of legacy OS and legacy OPROM messages. Configuration options are listed below.

- COM1 **Default**
- COM2
- COM3
- COM4
- COM5 (Pci Bus0,Dev0,Func0) (Disabled)

5.3.9 USB Configuration

Use the **USB Configuration** menu (**BIOS Menu 17**) to read USB configuration information and configure the USB settings.



BIOS Menu 17: USB Configuration

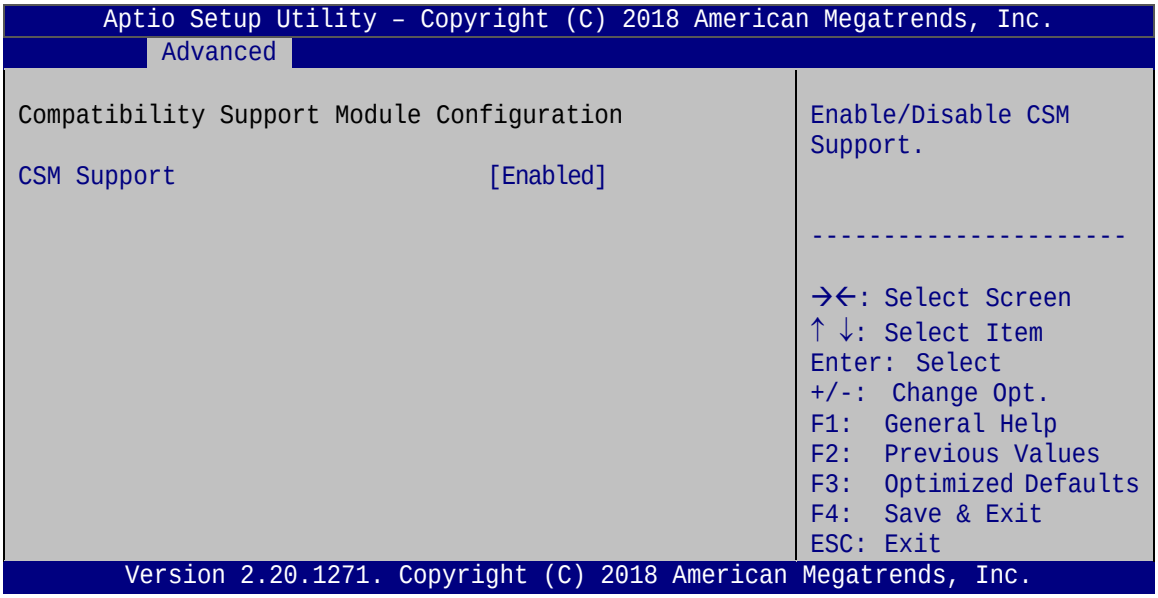
➔ **Legacy USB Support [Enabled]**

Use the **Legacy USB Support** BIOS option to enable USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

➔	**Enabled**	**DEFAULT**	Legacy USB support enabled
➔	**Disabled**		Legacy USB support disabled
➔	**Auto**		Legacy USB support disabled if no USB devices are connected

5.3.10 CSM Configuration

The **CSM Configuration** menu (**BIOS Menu 18**) configures the CSM (Compatibility Support Module) support.



BIOS Menu 18: CSM Configuration

➔ **CSM Support [Enabled]**

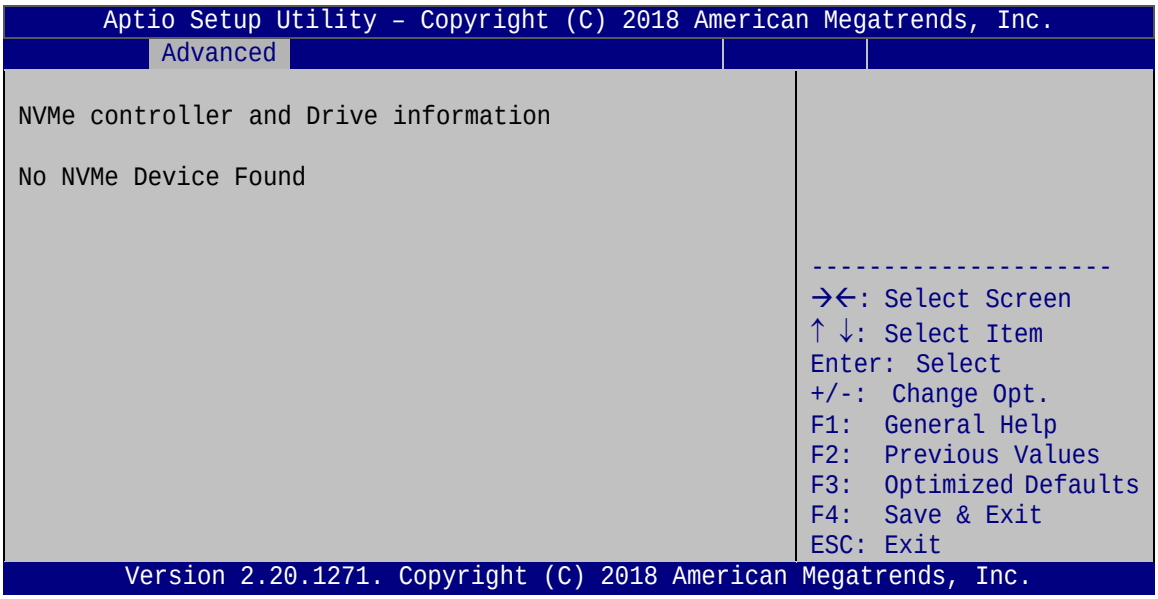
Use the **CSM Support** option to enable or disable CSM support.

➔ **Disabled** Disable CSM support.

➔ **Enabled** **DEFAULT** Enable CSM support.

5.3.11 NVMe Configuration

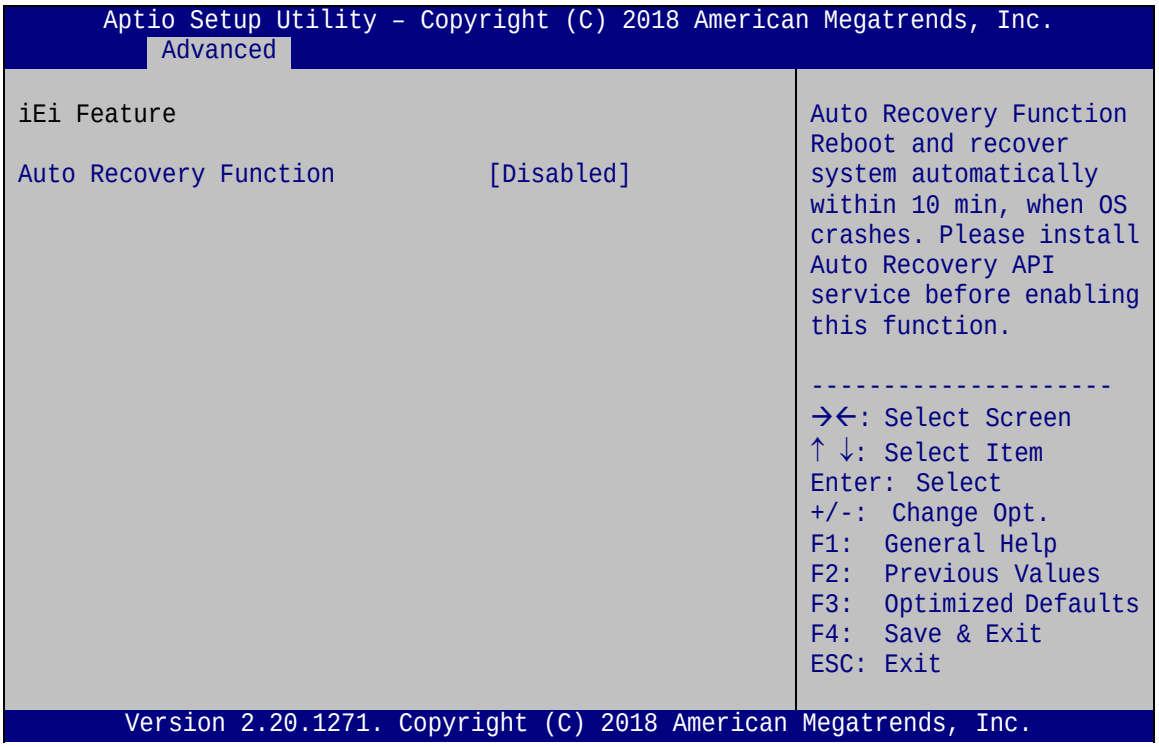
Use the **NVMe Configuration** (**BIOS Menu 19**) menu to display the NVMe controller and device information.



BIOS Menu 19: NVMe Configuration

5.3.12 iEi Feature

Use the **iEi Feature** menu (**BIOS Menu 20**) to configure One Key Recovery function.



BIOS Menu 20: iEi Feature

➔ **Auto Recovery Function [Disabled]**

Use the **Auto Recovery Function** BIOS option to enable or disable the auto recovery function of the IEI One Key Recovery.

➔ **Disabled** **DEFAULT** Auto recovery function disabled

➔ **Enabled** Auto recovery function enabled

5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 21**) to access the PCH IO and System Agent (SA) configuration menus.

WARNING!

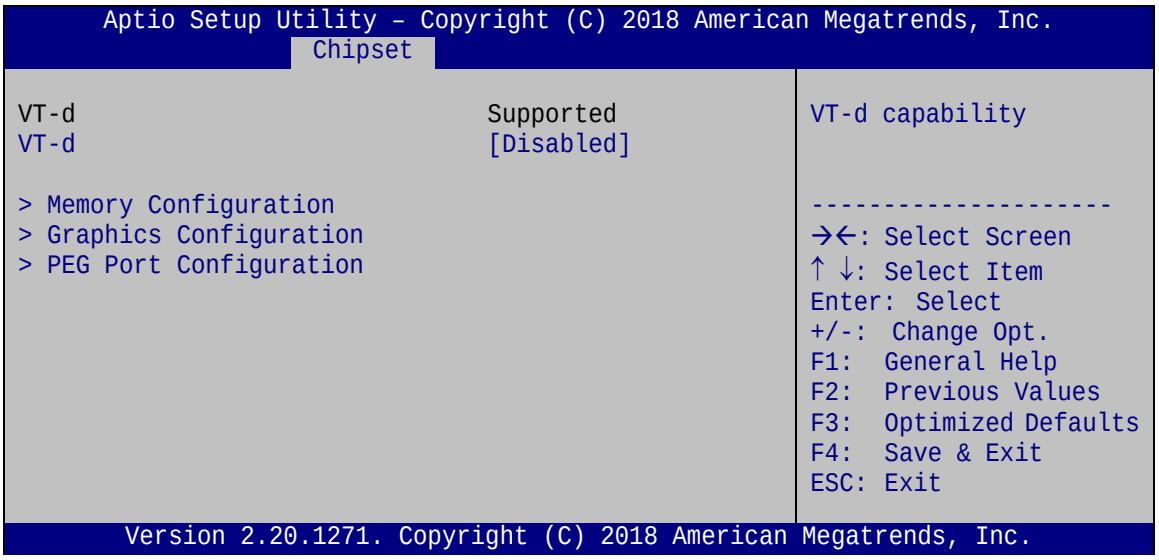
Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.

```
      Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
  Main    Advanced  Chipset  Security    Boot    Save & Exit

> System Agent (SA) Configuration                System Agent (SA)
> PCH-IO Configuration                           Parameters

                                                 ---------------------
                                                 →←: Select Screen
                                                 ↑ ↓: Select Item
                                                 Enter:  Select
                                                 +/-:  Change Opt.
                                                 F1:   General Help
                                                 F2:   Previous Values
                                                 F3:   Optimized Defaults
                                                 F4:   Save & Exit
                                                 ESC:  Exit
        Version 2.20.1271. Copyright (C) 2018 American Megatrends, Inc.
```

BIOS Menu 21: Chipset

5.4.1 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 22**) to configure the System Agent (SA) parameters.



BIOS Menu 22: System Agent (SA) Configuration

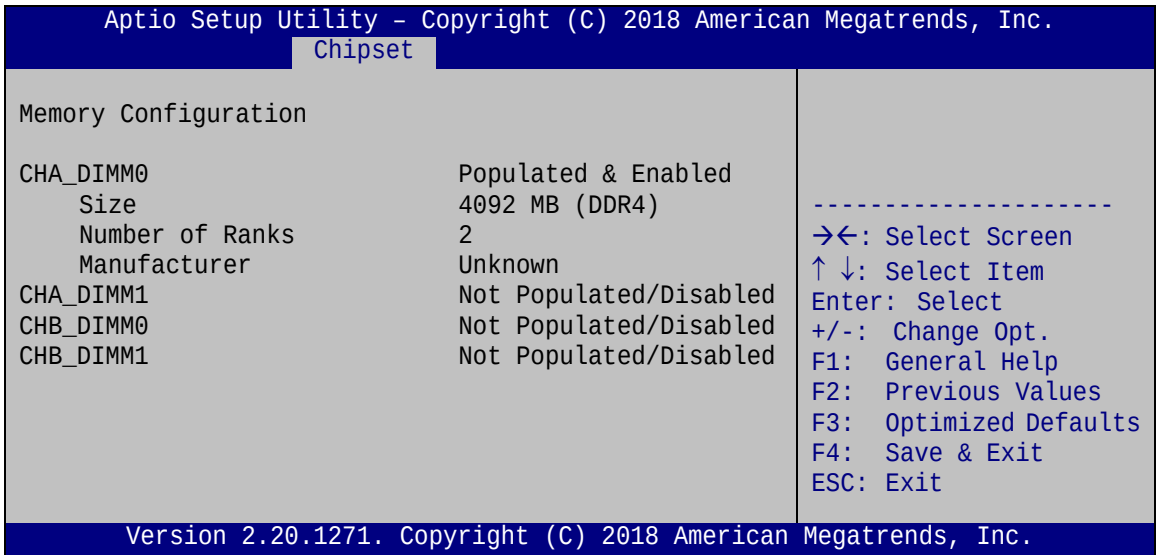
➔ **VT-d [Disabled]**

Use the **VT-d** option to enable or disable VT-d capability.

➔	**Disabled**	**DEFAULT**	Disables VT-d capability.
➔	**Enabled**		Enables VT-d capability.

5.4.1.1 Memory Configuration

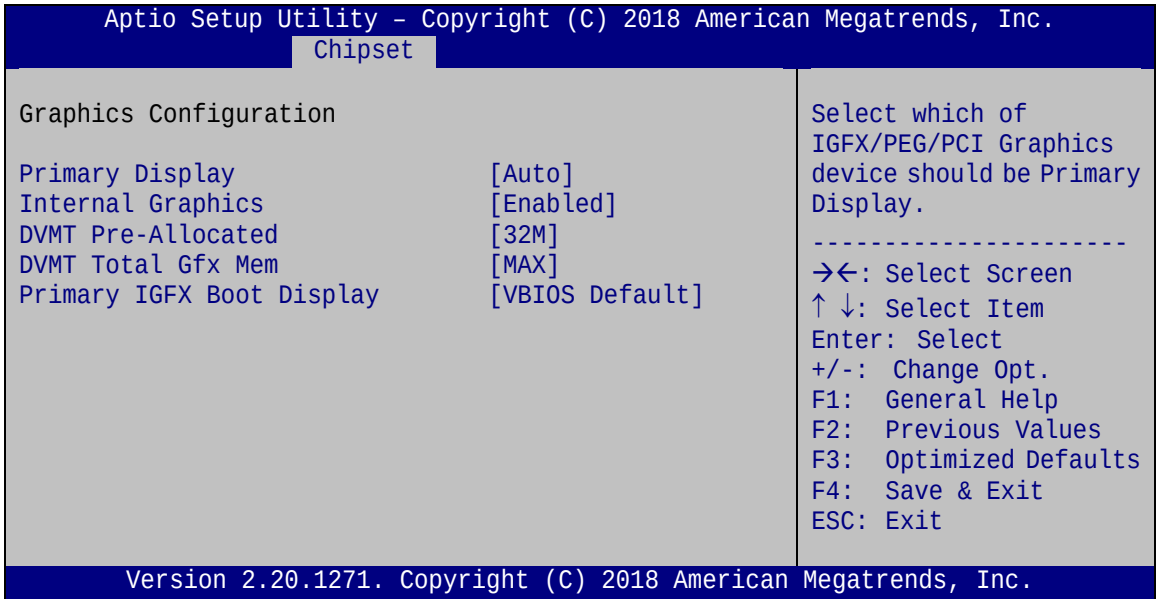
Use the **Memory Configuration** submenu (**BIOS Menu 23**) to view memory information.



BIOS Menu 23: Memory Configuration

5.4.1.2 Graphics Configuration

Use the **Graphics Configuration** (**BIOS Menu 24**) menu to configure the video device connected to the system.



BIOS Menu 24: Graphics Configuration

➔ **Primary Display [Auto]**

Use the **Primary Display** option to select the primary graphics controller the system uses. The following options are available:

- Auto **Default**
- IGFX
- PEG
- PCIe

➔ **Internal Graphics [Enabled]**

Use the **Internal Graphics** option to keep IGFX enabled basing on the setup options. The following options are available:

- Auto
- Disabled
- Enabled **Default**

➔ **DVMT Pre-Allocated [32M]**

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

- 32M **Default**
- 64M

➔ **DVMT Total Gfx Mem [MAX]**

Use the **DVMT Total Gfx Mem** option to select DVMT5.0 total graphic memory size used by the internal graphic device. The following options are available:

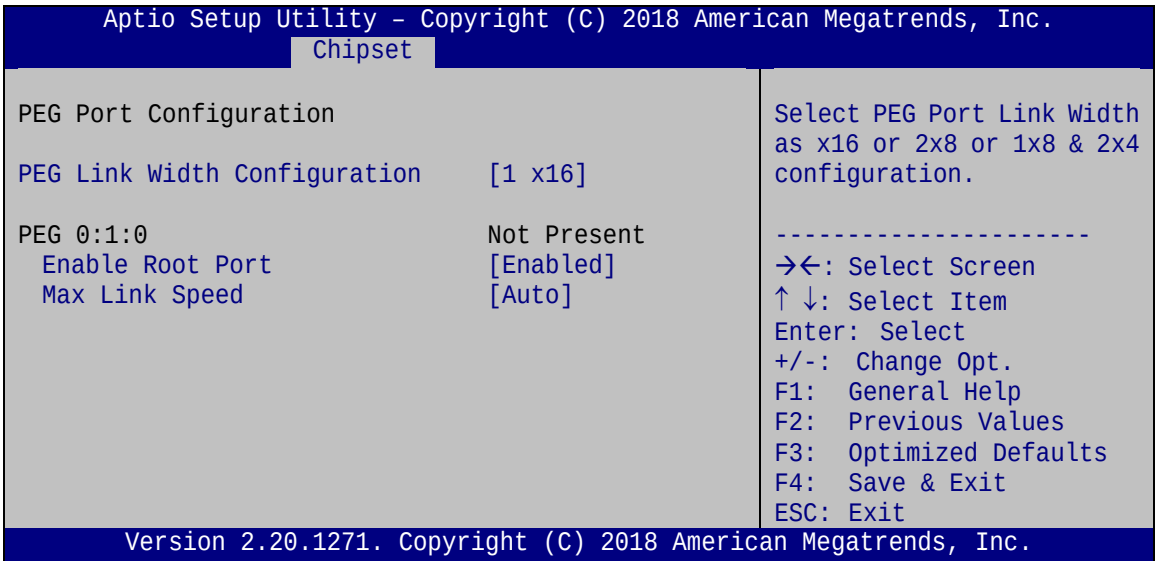
- 128M
- 256M
- MAX **Default**

➔ **Primary IGFX Boot Display [VBIOS Default]**

Use the **Primary IGFX Boot Display** option to select the display device used by the system when it boots. Configuration options are listed below.

- VBIOS Default **Default**
- CRT
- HDMI-C

5.4.1.3 PEG Port Configuration



BIOS Menu 25: PEG Port Configuration

➔ **PEG Link Width Configuration [1 x16]**

Use the **PEG Link Width Configuration** option to configure the PCIe x16 channel mode on the backplane.

➔ **1 x16**	**DEFAULT**	Sets the PCIe x16 link width as one PCIe x16 slot
➔ **2 x8**		Sets the PCIe x16 link width as two PCIe x8 slots
➔ **1 x8, 2 x4**		Sets the PCIe x16 link width as one PCIe x8 and two PCIe x4 slots

➔ **Enable Root Port [Enabled]**

Use the **Enable Root Port** option to enable or disable the PCI Express (PEG) controller.

➔ **Disabled**		Disables the PCI Express (PEG) controller.
➔ **Enabled**	**DEFAULT**	Enables the PCI Express (PEG) controller.

➔ **Max Link Speed [Auto]**

Use the **Max Link Speed** option to select the maximum link speed of the PCI Express slot.

The following options are available:

- Auto **Default**
- Gen1
- Gen2
- Gen3

5.4.2 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 26**) to configure the PCH parameters.

```
Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
                    Chipset

Auto Power Button Status          [Disable (ATX)]
Restore AC Power Loss             [Last State]

> PCI Express Configuration
> SATA And RST Configuration
> HD Audio Configuration

Power Saving Function(ERP)        [Disabled]
USB Power SW1                     [+5V DUAL]
USB Power SW2                     [+5V DUAL]

Select AC power state
when power is re-applied
after a power failure.

---------------------
→←: Select Screen
↑ ↓: Select Item
Enter:  Select
+/-:  Change Opt.
F1:  General Help
F2:  Previous Values
F3:  Optimized Defaults
F4:  Save & Exit
ESC:  Exit

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```

BIOS Menu 26: PCH-IO Configuration

➔ **Restore AC Power Loss [Last State]**

Use the **Restore AC Power Loss** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system.

➔ **Power Off**		The system remains turned off
➔ **Power On**		The system turns on
➔ **Last State**	**DEFAULT**	The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

➔ **Power Saving Function(ERP) [Disabled]**

Use the **Power Saving Function(ERP)** BIOS option to enable or disable the power saving function.

➔ **Disabled**	**DEFAULT**	Power saving function is disabled.
➔ **Enabled**		Power saving function is enabled. It will reduce power consumption when the system is off.

➔ **USB Power SW1 [+5V DUAL]**

Use the **USB Power SW1** BIOS option to configure whether to provide power to the four corresponding USB connectors (**Table 5-2**) when the system is in S3/S4 sleep state. This option is valid only when the above **Power Saving Function (ERP)** BIOS option is disabled.

➔ **+5V**		Sets the USB power source to +5V
➔ **+5V DUAL**	**DEFAULT**	Sets the USB power source to +5V dual

➔ **USB Power SW2 [+5V DUAL]**

Use the **USB Power SW1** BIOS option to configure whether to provide power to the four corresponding USB connectors (**Table 5-2**) when the system is in S3/S4 sleep state. This option is valid only when the above **Power Saving Function (ERP)** BIOS option is disabled.

➔ **+5V** Sets the USB power source to +5V

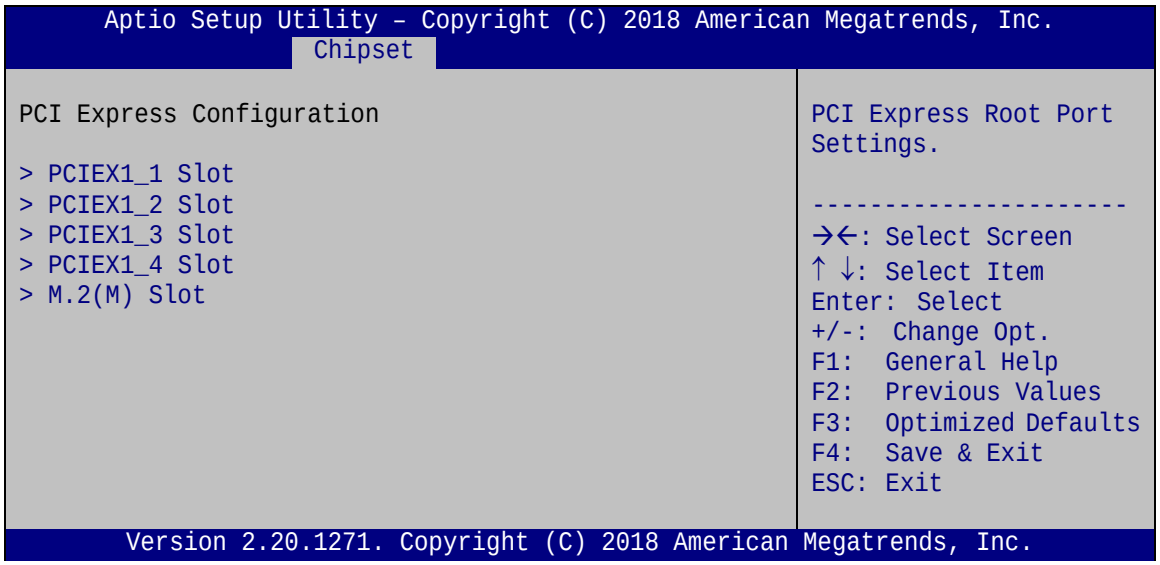
➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual

BIOS Options	Configured USB Ports
USB Power SW1	USB3_1 (external USB 3.1 Gen 1 port) USB3_2 (external USB 3.1 Gen 1 port) USB3 (internal USB 2.0 port, Type A)
USB Power SW2	USB1 (internal USB 2.0 ports) USB2 (internal USB 2.0 ports) USB4 (internal USB 2.0 ports) USB3-1 (internal USB 3.1 Gen 1 ports)

Table 5-2: BIOS Options and Configured USB Ports

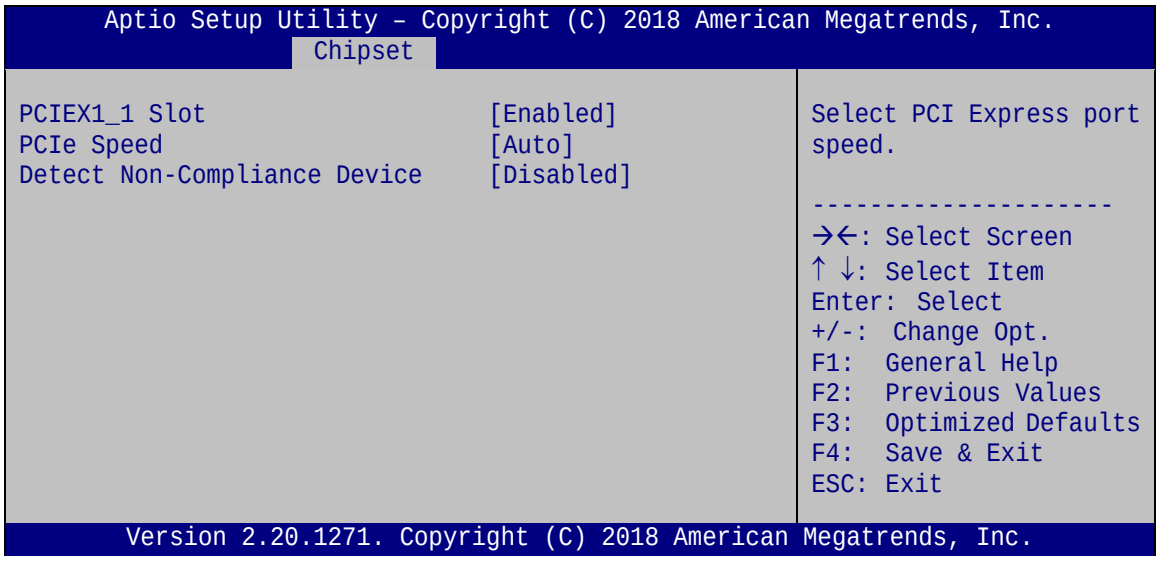
5.4.2.1 PCI Express Configuration

Use the **PCI Express Configuration** menu (**BIOS Menu 27**) to configure the PCI Express and M.2 slots.



BIOS Menu 27: PCI Express Configuration

5.4.2.1.1 PCIEX1 Slot/M.2 Slot



BIOS Menu 28: PCIEX1 Slot/M.2 Slot

➔ **PCIe Speed [Auto]**

Use this option to select the support type of the PCI Express slots. The following options are available:

- Auto **Default**
- Gen1
- Gen2
- Gen3

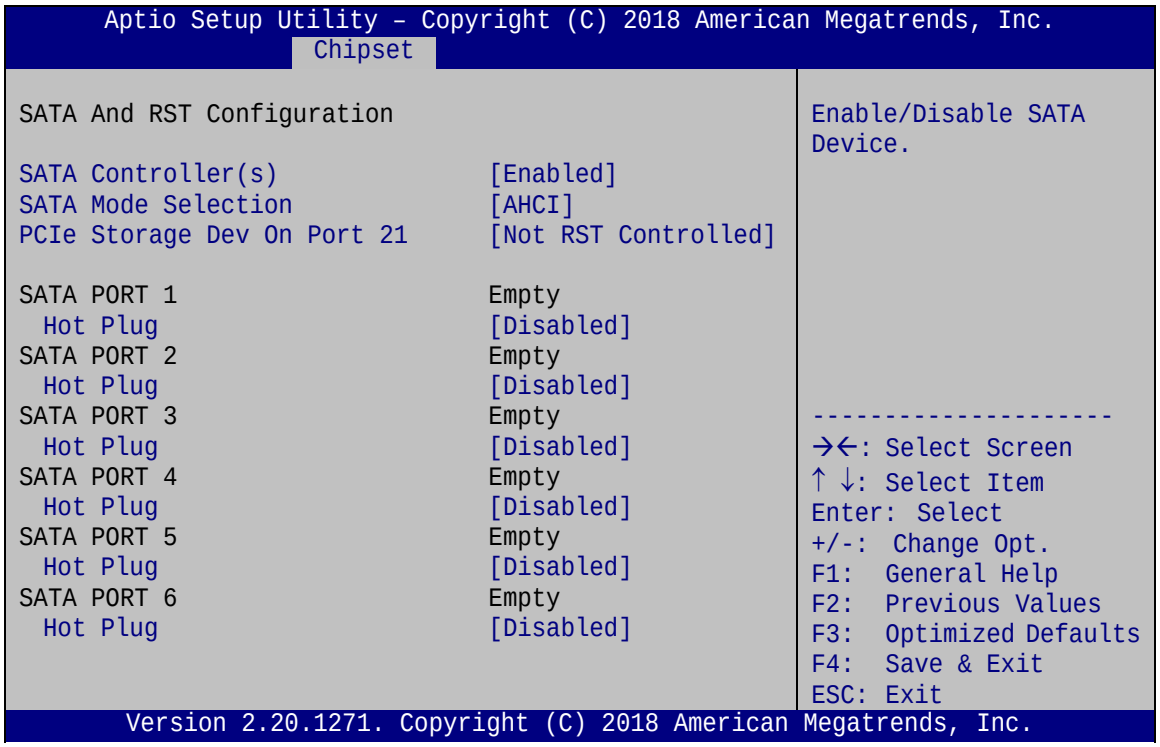
➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to enable or disable detecting if a non-compliance PCI Express device is connected to the PCI Express slot.

➔ **Disabled**	**DEFAULT**	Disables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.
➔ **Enabled**		Enables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.

5.4.2.2 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 29**) to change and/or set the configuration of the SATA devices installed in the system.



BIOS Menu 29: SATA Configuration

➔ **SATA Controller(s) [Enabled]**

Use the **SATA Controller(s)** option to configure the SATA controller(s).

➔ **Enabled** **DEFAULT** Enables the on-board SATA controller(s).

➔ **Disabled** Disables the on-board SATA controller(s).

➔ **SATA Mode Selection [AHCI]**

Use the **SATA Mode Selection** option to determine how the SATA devices operate.

➔ **AHCI**	**DEFAULT**	Configures SATA devices as AHCI device.
➔ **Intel RST Premium With Intel Optane System Acceleration**		Configures SATA devices to the Intel RST Premium With Intel Optane System Acceleration mode.

➔ **PCIe Storage Dev On Port 21**

Use the **PCIe Storage Dev On Port 21** option to enable or disable RST PCIe storage remapping which is only supported by UEFI.

➔ **RST Controlled**		Enables RST PCIe storage remapping. (*CSM Support* option must be disabled and *UEFI Boot* option must be enabled.)
➔ **Not RST Controlled**	**DEFAULT**	Disables RST PCIe storage remapping.

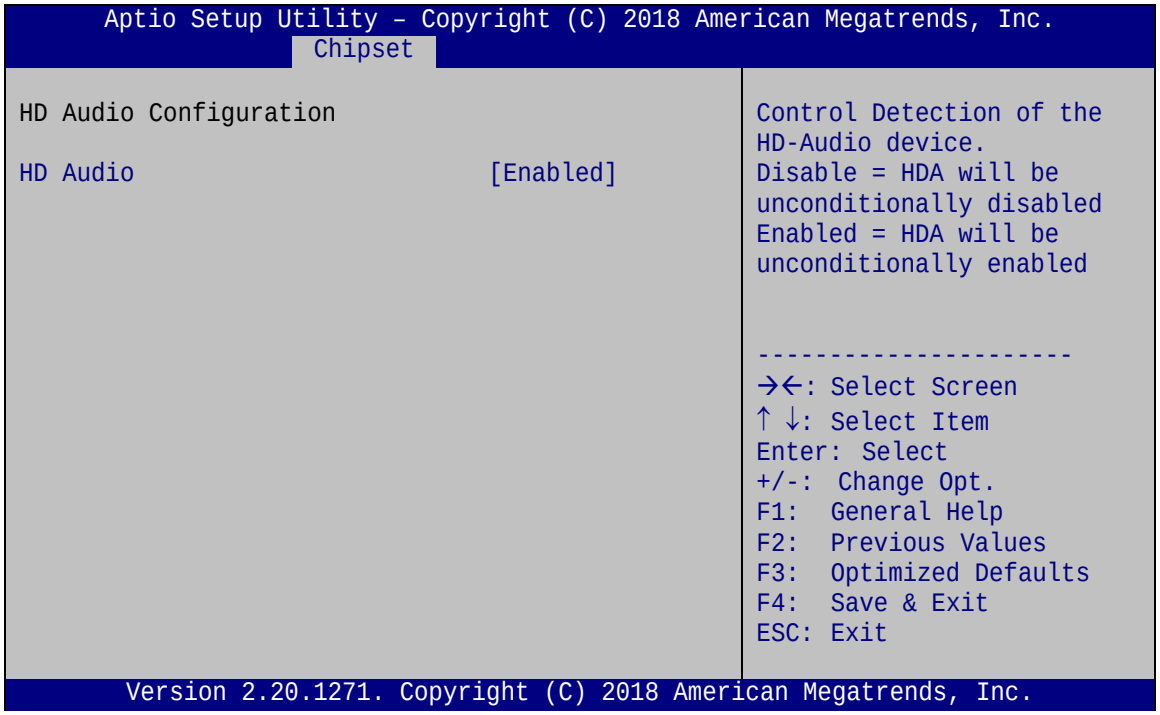
➔ **Hot Plug**

Use the **Hot Plug** option to enable or disable the hot plug function.

➔ **Disabled**	**DEFAULT**	Disables the hot plug function.
➔ **Enabled**		Enables the hot plug function.

5.4.2.3 HD Audio Configuration

Use the **HD Audio Configuration** menu (**BIOS Menu 30**) to configure the PCH Azalia settings.



BIOS Menu 30: HD Audio Configuration

➔ **HD Audio [Enabled]**

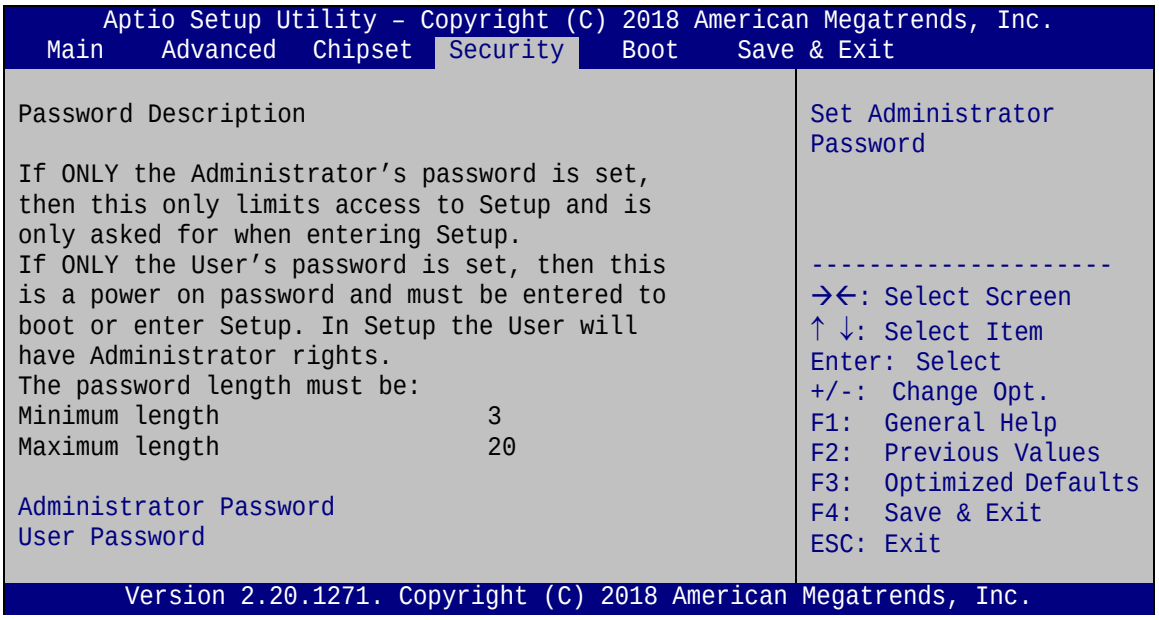
Use the **HD Audio** option to enable or disable the High Definition Audio controller.

➔ **Disabled** The onboard High Definition Audio controller is disabled.

➔ **Enabled** **DEFAULT** The onboard High Definition Audio controller is enabled.

5.5 Security

Use the **Security** menu (**BIOS Menu 31**) to set system and user passwords.



BIOS Menu 31: Security

➔ **Administrator Password**

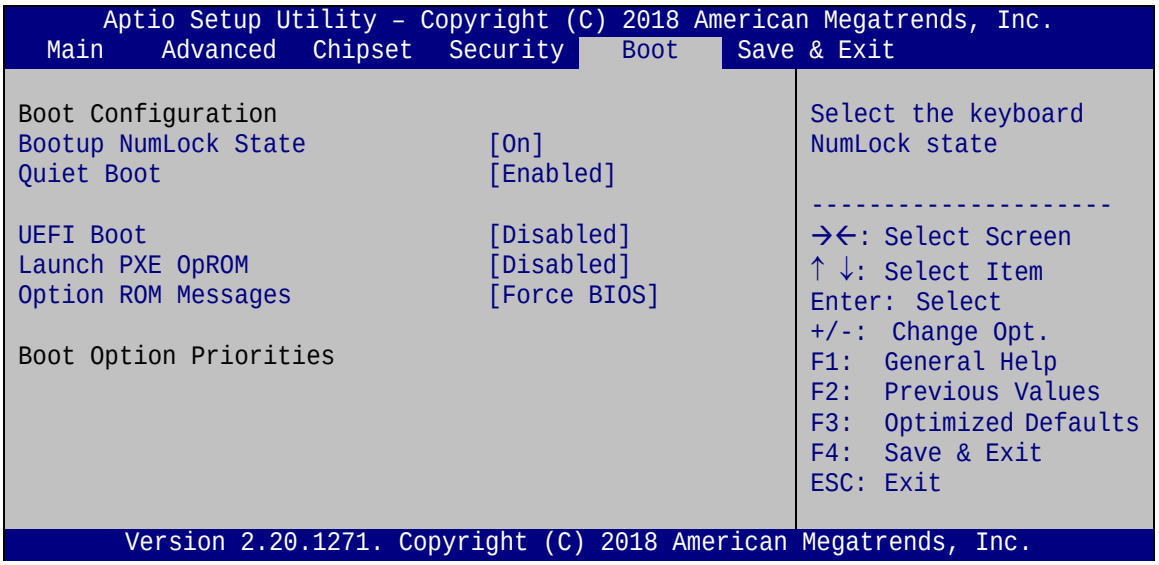
Use the **Administrator Password** to set or change a administrator password.

➔ **User Password**

Use the **User Password** to set or change a user password.

5.6 Boot

Use the **Boot** menu (**BIOS Menu 32**) to configure system boot options.



BIOS Menu 32: Boot

➔ **Bootup NumLock State [On]**

Use the **Bootup NumLock State** BIOS option to specify if the number lock setting must be modified during boot up.

➔ **On** **DEFAULT** Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.

➔ **Off** Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.

➔ **Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

➔	**Disabled**		Normal POST messages displayed
➔	**Enabled**	**DEFAULT**	OEM Logo displayed instead of POST messages

➔ **UEFI Boot [Disabled]**

Use the **UEFI Boot** option to enable or disable to boot from the UEFI devices.

➔	**Disabled**	**DEFAULT**	Boot from UEFI devices is disabled.
➔	**Enabled**		Boot from UEFI devices is enabled.

➔ **Launch PXE OpROM [Disabled]**

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

➔	**Disabled**	**DEFAULT**	Ignore all PXE Option ROMs
➔	**Enabled**		Load PXE Option ROMs.

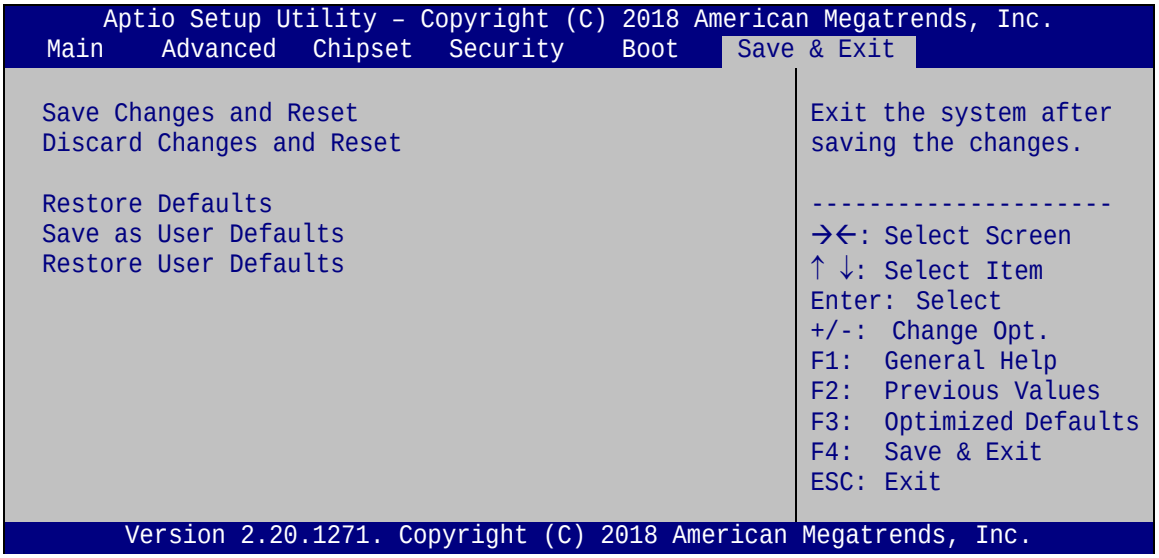
➔ **Option ROM Messages [Force BIOS]**

Use the **Option ROM Messages** option to set the Option ROM display mode.

➔	**Force BIOS**	**DEFAULT**	Sets display mode to force BIOS.
➔	**Keep Current**		Sets display mode to current.

5.7 Save & Exit

Use the **Safe & Exit** menu (**BIOS Menu 33**) to load default BIOS values, optimal failsafe values and to save configuration changes.



BIOS Menu 33: Save & Exit

➔ **Save Changes and Reset**

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

➔ **Discard Changes and Reset**

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

➔ **Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

➔ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

➔ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

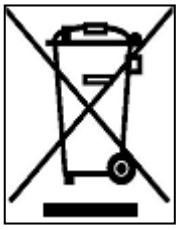
Product Disposal

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union–If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union–The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

BIOS Options

Below is a list of BIOS configuration options in the BIOS chapter.

Appendix

D

Terminology

AC '97	Audio Codec 97 (AC'97) refers to a codec standard developed by Intel® in 1997.
ACPI	Advanced Configuration and Power Interface (ACPI) is an OS-directed configuration, power management, and thermal management interface.
AHCI	Advanced Host Controller Interface (AHCI) is a SATA Host controller register-level interface.
ATA	The Advanced Technology Attachment (ATA) interface connects storage devices including hard disks and CD-ROM drives to a computer.
ARMD	An ATAPI Removable Media Device (ARMD) is any ATAPI device that supports removable media, besides CD and DVD drives.
ASKIR	Amplitude Shift Keyed Infrared (ASKIR) is a form of modulation that represents a digital signal by varying the amplitude ("volume") of the signal. A low amplitude signal represents a binary 0, while a high amplitude signal represents a binary 1.
BIOS	The Basic Input/Output System (BIOS) is firmware that is first run when the computer is turned on and can be configured by the end user
CODEC	The Compressor-Decompressor (CODEC) encodes and decodes digital audio data on the system.
CMOS	Complimentary metal-oxide-conductor is an integrated circuit used in chips like static RAM and microprocessors.
COM	COM refers to serial ports. Serial ports offer serial communication to expansion devices. The serial port on a personal computer is usually a male DB-9 connector.
DAC	The Digital-to-Analog Converter (DAC) converts digital signals to analog signals.
DDR	Double Data Rate refers to a data bus transferring data on both the rising and falling edges of the clock signal.
DMA	Direct Memory Access (DMA) enables some peripheral devices to bypass the system processor and communicate directly with the system memory.

DIMM	Dual Inline Memory Modules are a type of RAM that offer a 64-bit data bus and have separate electrical contacts on each side of the module.
DIO	The digital inputs and digital outputs are general control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.
EHCI	The Enhanced Host Controller Interface (EHCI) specification is a register-level interface description for USB 2.0 Host Controllers.
EIDE	Enhanced IDE (EIDE) is a newer IDE interface standard that has data transfer rates between 4.0 MBps and 16.6 MBps.
EIST	Enhanced Intel® SpeedStep Technology (EIST) allows users to modify the power consumption levels and processor performance through application software. The application software changes the bus-to-core frequency ratio and the processor core voltage.
FSB	The Front Side Bus (FSB) is the bi-directional communication channel between the processor and the Northbridge chipset.
GbE	Gigabit Ethernet (GbE) is an Ethernet version that transfers data at 1.0 Gbps and complies with the IEEE 802.3-2005 standard.
GPIO	General purpose input
HDD	Hard disk drive (HDD) is a type of magnetic, non-volatile computer storage device that stores digitally encoded data.
ICH	The Input/Output Control Hub (ICH) is an Intel® Southbridge chipset.
IrDA	Infrared Data Association (IrDA) specify infrared data transmission protocols used to enable electronic devices to wirelessly communicate with each other.
L1 Cache	The Level 1 Cache (L1 Cache) is a small memory cache built into the system processor.
L2 Cache	The Level 2 Cache (L2 Cache) is an external processor memory cache.
LCD	Liquid crystal display (LCD) is a flat, low-power display device that consists of two polarizing plates with a liquid crystal panel in between.

LVDS	Low-voltage differential signaling (LVDS) is a dual-wire, high-speed differential electrical signaling system commonly used to connect LCD displays to a computer.
POST	The Power-on Self Test (POST) is the pre-boot actions the system performs when the system is turned-on.
RAM	Random Access Memory (RAM) is volatile memory that loses data when power is lost. RAM has very fast data transfer rates compared to other storage like hard drives.
SATA	Serial ATA (SATA) is a serial communications bus designed for data transfers between storage devices and the computer chipsets. The SATA bus has transfer speeds up to 1.5 Gbps and the SATA II bus has data transfer speeds of up to 3.0 Gbps.
S.M.A.R.T	Self Monitoring Analysis and Reporting Technology (S.M.A.R.T) refers to automatic status checking technology implemented on hard disk drives.
UART	Universal Asynchronous Receiver-transmitter (UART) is responsible for asynchronous communications on the system and manages the system's serial communication (COM) ports.
UHCI	The Universal Host Controller Interface (UHCI) specification is a register-level interface description for USB 1.1 Host Controllers.
USB	The Universal Serial Bus (USB) is an external bus standard for interfacing devices. USB 1.1 supports 12Mbps data transfer rates and USB 2.0 supports 480Mbps data transfer rates.
VGA	The Video Graphics Array (VGA) is a graphics display system developed by IBM.

Appendix

E

Digital I/O Interface

E.1 Introduction

The DIO connector on the PCIE-Q370 is interfaced to GPIO ports on the Super I/O chipset. The digital inputs and digital outputs are generally control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.

NOTE:

For further information, please refer to the datasheet for the Super I/O chipset.

The BIOS interrupt call **INT 15H** controls the digital I/O.

INT 15H:

AH – 6FH	
Sub-function:	
AL – 8	:Set the digital port as INPUT
AL	:Digital I/O input value

E.2 Assembly Language Sample 1

```
MOV     AX, 6F08H       ;setting the digital port as input
INT     15H             ;
```

AL low byte = value

AH – 6FH	
Sub-function:	
AL – 9	:Set the digital port as OUTPUT
BL	:Digital I/O input value

E.3 Assembly Language Sample 2

```
MOV     AX, 6F09H       ;setting the digital port as output
MOV     BL, 09H         ;digital value is 09H
INT     15H             ;
```

Digital Output is 1001b

Appendix

F

Watchdog Timer

NOTE:

The following discussion applies to DOS environment. Contact IEI support or visit the IEI website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table F-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

NOTE:

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

EXAMPLE PROGRAM:

```
; INITIAL TIMER PERIOD COUNTER

;
W_LOOP:
;

        MOV     AX, 6F02H       ;setting the time-out value
        MOV     BL, 30          ;time-out value is 48 seconds
        INT     15H

;
; ADD THE APPLICATION PROGRAM HERE
;

        CMP     EXIT_AP, 1      ;is the application over?
        JNE     W_LOOP          ;No, restart the application

        MOV     AX, 6F02H       ;disable Watchdog Timer
        MOV     BL, 0           ;
        INT     15H

;
; EXIT ;
```

Appendix

G

Hazardous Materials Disclosure

The details provided in this appendix are to ensure that the product is compliant with the Peoples Republic of China (China) RoHS standards. The table below acknowledges the presences of small quantities of certain materials in the product, and is applicable to China RoHS only.

A label will be placed on each product to indicate the estimated "Environmentally Friendly Use Period" (EFUP). This is an estimate of the number of years that these substances would "not leak out or undergo abrupt change." This product may contain replaceable sub-assemblies/components which have a shorter EFUP such as batteries and lamps. These components will be separately marked.

Please refer to below table.

Part Name	Toxic or Hazardous Substances and Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
Housing	O	O	O	O	O	O
Display	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O
Battery	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011).

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011).

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	O	O	O	O	O	O
显示	O	O	O	O	O	O
印刷电路板	O	O	O	O	O	O
金属螺帽	O	O	O	O	O	O
电缆组装	O	O	O	O	O	O
风扇组装	O	O	O	O	O	O
电力供应组装	O	O	O	O	O	O
电池	O	O	O	O	O	O

O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T 11363-2006 (现由 GB/T 26572-2011 取代) 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 (现由 GB/T 26572-2011 取代) 标准规定的限量要求。